

Fabrication and Characterisation of Polyimide Multilayer Structures for MMICs

Tuyen V Vo, Lokesh Krishnamurthy, Robin Sloan and Ali A Rezazadeh
The Electromagnetic Centre for Microwave and mm-wave Design and Applications
Department of Electrical Engineering and Electronics, UMIST, Manchester, UK, M60 1QD

Abstract

In this paper the fabrication of novel multilayer monolithic microwave integrated circuit (MMIC) structures using polyimide as insulating dielectric layer has been described. The polyimide layer formation, curing and dry etching processes have been investigated in an attempt to obtain high quality dielectric layers suitable for MMICs applications. By employing this technique, MMIC design and circuit routings become much easier and conventional microstrip transmission lines and lumped passive components can be realised with effective use of the substrate material. In this paper, it is shown that MMIC coplanar waveguide (CPW) transmission lines with low characteristic impedance and edge offset broadside directional couplers can easily be designed using the multilayer technique. This implementation can avoid the well known current crowding effects on the conductor edges. Within the Ku and K band frequency range, circuits have been characterised and show good performances.

Keywords: GaAs Fabrication Technology, MMICs, Multilayer Circuits

Introduction

Conventional monolithic microwave integrated circuits (MMICs) use semi-insulating substrate GaAs to confine the electric field around the conductors and normally the back face of the substrate is moralised as ground. However there are several problems associated with this technology: firstly the microstrip lines and other MMIC components are designed with sizes scaled to the chip thickness. For a wafer thickness of about 100 to 200 μm , a similar component line features are required. With these feature sizes the gaps between the conductor lines must be kept large to avoid coupling; secondly for operation up to 12 GHz, devices and components can only be effectively grounded with through-substrate via holes. This makes the fabrication process complicated and the wafer thickness is limited to about 100 to 200 μm . These thin wafers put a requirement on the wafer sizes which can be handled safely and thus the

fabrication cost would be high; thirdly at the millimetric frequencies the via hole inductance becomes significant and can deteriorate the circuit performance [1, 2].

Due to the above problems, coplanar waveguide (CPW) structures have received much attention [1-5]. In CPW structures there is no need for the back face ground metal thus via holes can be avoided and wafer sizes will not be limited by this process. The chip thickness as thick as 600 μm can be used allowing larger wafer sizes to be employed. In addition, the individual component sizes are unlimited. These factors can greatly reduce the processing costs.

In this paper, we present the fabrication and characterisation of some novel multilayer MMIC structures. It is shown that a significant improvement can be achieved using multilayer structures compared with the conventional microstrip MMIC technique.

Multilayer Structure Fabrications

The multilayer structures in this work have been fabricated using three layers of metals and two layers of sandwich dielectrics. In realising these multilayer structures, several processing aspects have been studied including polyimide spin, curing, etching and metal contact formation. In the fabrication of these structures, different layers need to be interconnected properly through the etched windows of the polyimide insulating layers.

In this work polyimide was used to fabricate several CPW capacitors using a combination of two metals and a polyimide dielectric layer with the combination of Au(0.8 μ m)/PI(1.1 μ m)/Au(0.45 μ m)/GaAs(500 μ m).

Following the fabrication of test capacitors and the normal curing of the polyimide Current voltage measurements were made on various fabricated capacitors (figure 1). The results showed that the polyimide breakdown voltage is over 200V. This is corresponds to an electric field strength of about 2×10^6 V/cm which is considerable high enough for the design optimization of multilayer circuits.

In order to determine the dielectric constant of polyimide layer we have plot the variation of capacitances with the device areas for two cases: For when the first cure was performed (120C/120min) and for the additional cure process using similar curing condition. The capacitances were then measured at 1MHz with the 25mV signal level using HP4284 LCR meter and the results are given in figure 2. The first cure process gave a relative dielectric constant of 3.79 and the effect of additional cure was to reduce this value to only 3.69. The manufacture's specification for the dielectric constant is 2.9. However

the measured Q factor at 1MHz shows an improvement, as it increased from around 40 to 90, which means that better isolation of the polyimide has been achieved.

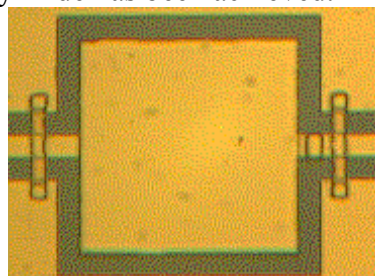


Figure 1: A micrograph of fabricated capacitor.

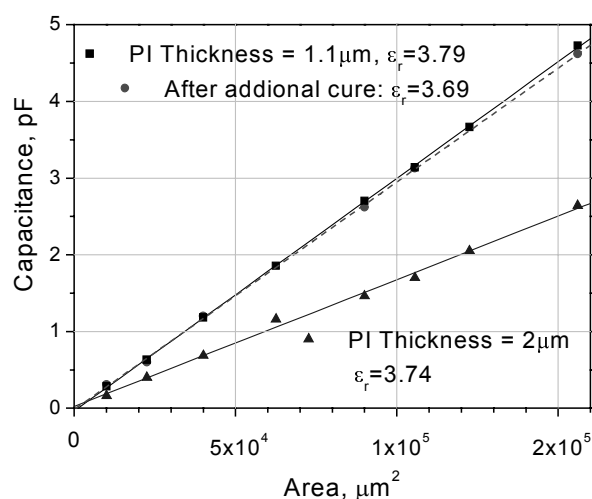


Figure 2: The variation of capacitances with the area. The data are shown for two set of capacitors: one with 1.1 μ m and the second one with 2 μ m polyimide layers.

The polyimide interconnection windows were formed by oxygen plasma reactive ion etching (RIE) through a photoresist protecting layer patterned using the lithography process. In order to optimise the polyimide etching process, different polyimide etching conditions had been tried including varying plasma power, chamber pressure and gas flow rate. An example of dry etching is shown in figure 6 where an edge coupler is fabricated

Microwave Characterisation

The fabricated multilayer structures are characterised at microwave frequencies using Cascade Microtech on-wafer probe station and a HP 8510B vector network analyser. Simulations were carried out using both Momentum and HFFS simulators.

CPW multilayer transmission lines

For the MMICs, low impedance transmission lines have been shown to be useful components, especially in matching networks [4,5]. In conventional MMICs, the transmission lines typically have a characteristic impedance of 40-100Ω, while the microwave device themselves have a much lower input impedance. This imposes a requirement on the transmission line design, since low impedance lines can not be readily used. To design a coplanar transmission line with extra low impedance requires a very narrow slot between the conductors. At high frequency, the signal loss at the edge of the conductor is high due to the current crowding effects. Various methods to overcome this problem and to realise low loss lines and small compact microstrip lines have been proposed. In this study it is demonstrated that by employing multilayer structures transmission line can easily be constructed. This was achieved by proper design of the transmission line structure allowing the current to be effectively dispersed within the conductor thus eliminating the current crowding effect.

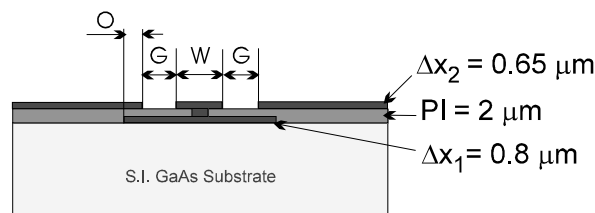


Figure 3: Cross-section view of an edge CPW transmission line fabricated on S.I GaAs substrate

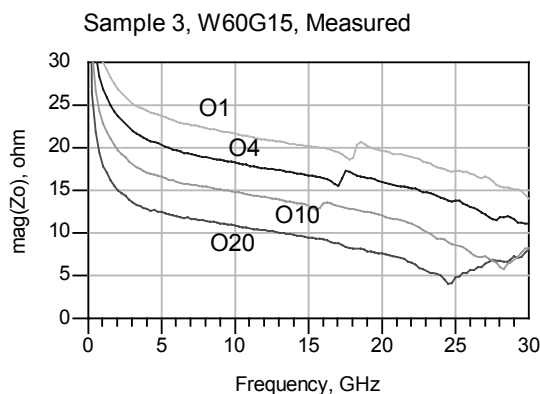


Figure 4: The variation of measured impedance with frequency for various overlap design as in figure 3.

Figure 3 and 4 clearly shows that with appropriate overlap design of transmission lines various impedance can be achieved for circuit matching. At 20GHz when the overlap is only 1μm the impedance is as high as 20Ω. This can be reduced by simply increasing the overlap to 20μm reducing the impedance to about 8Ω.

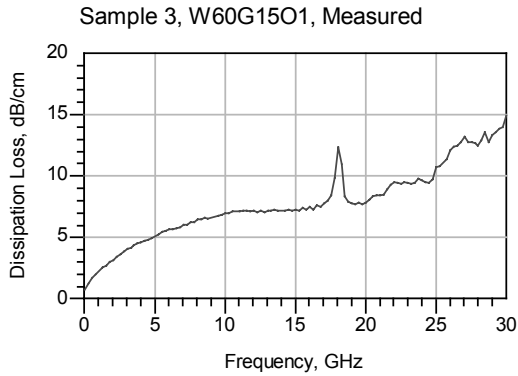


Figure 5: Measured dissipation loss as a function of frequency for various overlap design as in figure 3.

It is useful to plot the variation of dissipation factor with frequency for this structure. It is very common to consider the use of two-port network where the reflected power from the input is $1 - |S_{11}|^2$. The output power can be approximated as $|S_{21}|^2$. Therefore the dissipation loss can be approximated as:

$$Loss = l * 10 \log \frac{1 - |S_{11}|^2}{|S_{21}|^2} \quad (1)$$

We have used equation (1) to plot the dissipation factor as given in figure 5.

CPW directional couplers

Transmission line couplers are commonly used in balanced amplifiers, phase shifters and mixers for power splitting or combining [5]. In this study a combination of both edge coupling and offset parallel broadside coupling has been designed employing the multilayer technique. An edge CPW coupler has been designed with the following construction:

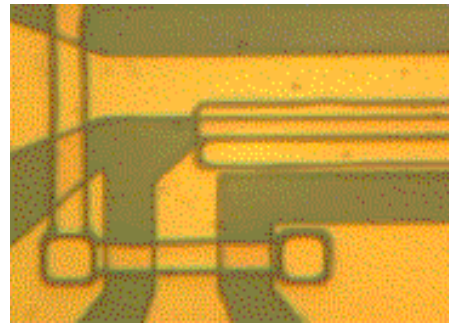


Figure 6: A micrograph of fabricated directional coupler showing the top view of the Au metal and the interconnect to the lower metal contact via the polyimide layer. This device has the following structure Au(0.65um)/Polyimide (2um)/Au(0.8um)/GaAs (600um).

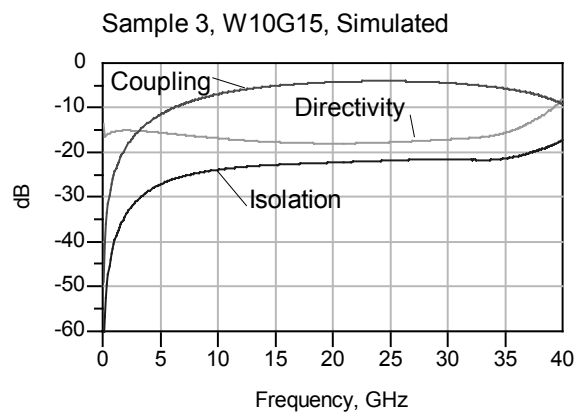


Figure7: Simulation of coupler given in figure 6.

The Momentum simulator in the ADS has been used to simulate the performance this coupler. Figure 6 shows the simulation of an edge coupler with CPW multilayer circuit technology.

The results suggested that a coupling factor of -4dB has been achieved in this design with a directivity of about 18dB the isolation is 22dB and the phase shift of about 90°.

Conclusion

Multilayer structures for MMIC were designed, fabricated and tested. It was shown that by appropriate polyimide processing and proper control of dry etching, one can achieve good dielectric for interlayer insulating material in MMIC circuits. Using this technique a variety of novel multilayer MMIC components can be designed with good performance to meet various circuit requirements. In this study, an edge CPW transmission line and a directional coupler have been designed, fabricated and tested. It is shown that by using multilayer technique these couplers can be realised with compact sizes while maintaining a good matching properties. These circuit demonstrators present a potential application for multilayer techniques in the MMIC industry.

Acknowledgment

The authors would like to thank EMRS DTC Board for their encouragement and the financial support for this work.

Reference

1. Ogawa H, Hasegawa H, Banba S and Nakamoto H, 1991, IEEE MTT-S Digest, p1067.
2. Sanchez-hernandez D, Wang D H, , Rezazadeh A A and Robertson I D, 1996, IEEE Microwave Theory and Techniques, Vol. 44, No. 9, September, 1590-1593.
3. Budimir D, Robertson I D, Khalid A H and Rezazadeh A A, 1998, Microwave and Optical Technology Letters, Volume 17, No.2, 125-128.
4. Tokumitsu T, Hiraoka T, Nakamoto H and Takenaka T, 1990, IEEE-MTT-S, p.831.
5. Wen C P, 1970, IEEE Trans., Microwave Theory Tech., MTT-18, no. 6, 318-322.