The Application of Time to Digital Converters to ESM Systems

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Abstract

Research into high-energy physics has driven the development of Time-to-Digital Converters (TDCs) that measure the relative timing of pulse edges. It is proposed that TDC technology may be incorporated into future low-cost ESM systems, for example in UAVs, to provide a direction finding capability using time difference of arrival (TDOA) techniques. Commercially available single chip TDCs have been identified that have sufficient precision to be used in short baseline TDOA systems, providing rms DF accuracy of a few degrees at moderate ranges.

Keywords: Direction Finding; Time-to-Digital Converters; TDOA; UAV

Introduction

There are a number of commonly used techniques for direction finding, including amplitude comparison, interferometery, frequency difference of arrival and time difference of arrival. It is suggested that time difference of arrival (TDOA) has a number of advantages over the other techniques, particularly when a low-cost system suitable for UAV installation is considered.

TDOA systems require simpler hardware, do not suffer from ambiguities, may be very broad-band, and, if based on pulse leading edges, are immune to multipath. The main limitation of TDOA, at least in the form considered here, is that it relies on the emitter being pulsed rather than CW. Hence it is more applicable to radar than to communications ESM.

Research into high-energy physics has driven the development of integrated timing devices, or Time-to-Digital Converters (TDCs), that measure the relative timing of pulse edges. It is proposed that TDC technology may be used in low-cost TDOA DF systems for small platforms such as UAVs or land vehicles.

Theoretical Assessment of the TDOA Technique

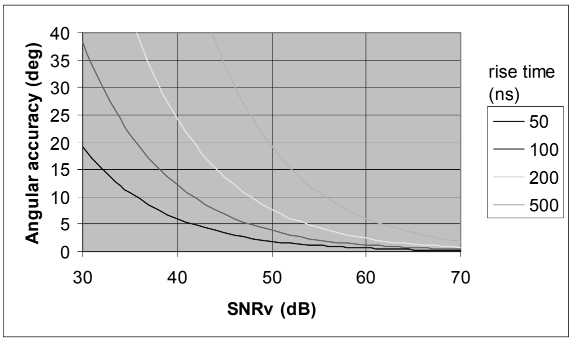
Traditionally TDOA DF has been performed using long baselines, and hence fairly low resolution is required in the time measurement. However, a UAV or land vehicle installation constrains the baseline to a few metres at most, demanding correspondingly greater accuracy. For example, to obtain an rms error of 2° on boresight, using a 2m baseline requires a TDOA rms error of 230ps.

For a single pulse TDOA measurement, the rms bearing error is given by:

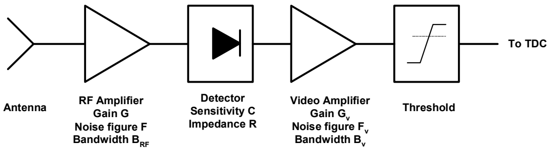
$$\sigma_\theta = \frac{ct_r\sqrt{2}}{L\cos\theta\sqrt{SNR_V}}$$

Where t_r is the pulse rise time, L is the antenna baseline and SNR_V is the video signal to noise ratio. It is noted that in many applications it is possible to average over a number of pulses to give improved accuracy.

Given the receiver design, and some fairly readily available parameters of the threat radar, it is quite straightforward to calculate the SNR. However, information on radar pulse rise times is rather harder to obtain. The limited data available suggests that rise times from 50 to 500 ns may typically be encountered [1]. Depending on the pulse rise time, useful DF performance (e.g. better than 5° rms from a single pulse) requires a video SNR of 40 to 60 dB.



Rise time and SNR dependence



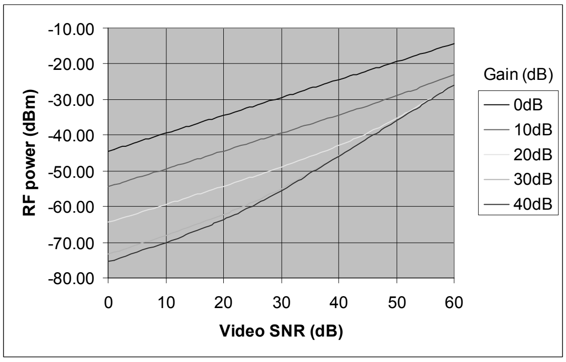
Receiver Architecture

If the receiver architecture consists of a square-law detector with an RF preamplifier, the video SNR can be related to the received RF power level:

$$P_R = kTFB_V SNR_V \left[2 + \sqrt{4 + \frac{2B_{RF} - B_V + A/(GF)^2}{B_V SNR_V}} \right]$$

where the diode parameter $A = \dfrac{4F_V R}{kTC^2}$

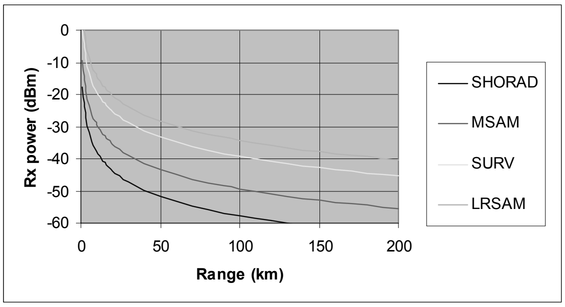
It will be assumed that the system covers the frequency band 2-18 GHz, and has a video bandwidth of 20 MHz. Typical values for the other parameters were taken from manufacturers' data sheets.



Performance of square law detector with pre-amplifier

It is observed that for the SNR region of interest, around 20 dB of RF gain is required to approach a noise limited (rather than detector limited) performance. In this case RF power of -45 to -25 dBm is seen to be needed to give 40-60 dB video SNR.

Assuming that the DF system has omni-directional antennas, the received power from a number of representative threat radars has been calculated. It is observed that the range at which adequate power is received varies from a few km up to 100 km or more. It should be emphasized that these figures relate to main beam intercepts, which for scanning radars with narrow beams may be comparatively infrequent. Assuming 30-40 dB sidelobes, the operating range for sidelobe intercepts will be less by a factor of between 30 and 100, hence useful DF performance is only possible against long range radars.



Power received from representative radars

TDC Technology

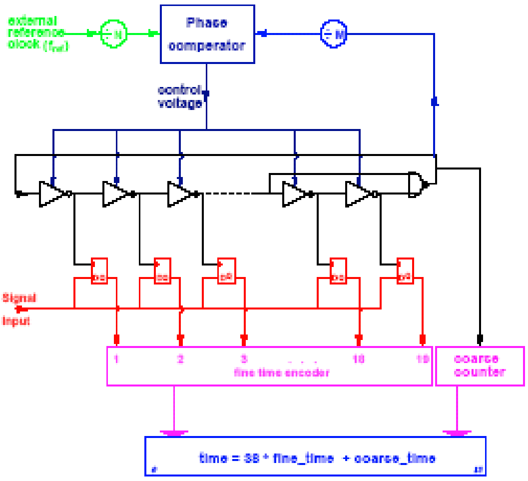
Accurate measurement of time intervals is of importance in a number of fields, for example particle physics and Laser Range Finding (LRF), hence considerable effort has been expended on the problem.

One approach is to first convert the time interval into a voltage, for example by charging a capacitor using a constant current source. Such a device is known as a Time to Analogue Converter (TAC). The TAC output can then be converted into a digital form using a conventional Analogue to Digital Converter (ADC). There are a number of disadvantages to this technique, and a direct Time to Digital Converter (TDC) is to be preferred.

Simple digital counting techniques are limited by the clock speed of the counter, which with current technology gives around 1ns resolution. However a digital counter can be combined with another technique to measure the part cycles at the end of the time interval. Although there are a number of variations, the techniques can be divided into those that involve an analogue stage, and those that are purely digital.

One very powerful technique is the use of digital delay lines. The signal is fed to a number of D-type latches, which have clocks with progressively increasing time delays. This enables the signal arrival time to be determined to a resolution given by the gate propagation time, which is typically of the order 100 to 200ps. The great advantage of this approach is that the TDC can be constructed using a standard digital CMOS process. Since the gate delay varies with temperature and supply voltage, performance is improved by the use of delay locked loop or phase locked loop techniques.

Although a number of development programmes have been reported in the literature, it appears that at the time of writing the only commercially available TDC chips are those manufactured by ACAM, originally for use at CERN [2].

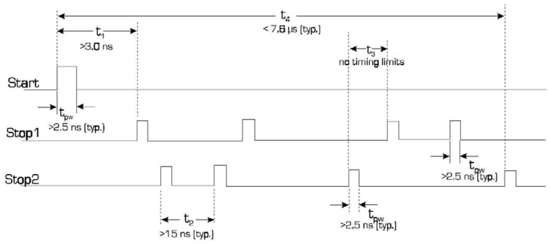


ACAM TDC using PLL technique

While this single-source situation may cause some concern, this is alleviated by the number of successful prototypes that have been reported, and the fact that a standard CMOS process is used. Also, one team has reported a successful implementation of a TDC using a standard FPGA [3].

ACAM produce two TDCs, the TDC-F1, which is the device developed for CERN, having 8 timing channels with nominally 120ps resolution, or 4 channels with 60ps resolution. The other device is the TDC-GP1, which has 2 channels with nominally 250ps resolution, or 1 channel with 125ps resolution. The devices operate over the extended temperature range -40° to +85°C and are currently priced at around €125 and €25 respectively.

The TDC-GP1 is implemented in a 0.8μm CMOS process and offers two timing channels with a common start and independent stop inputs. The chip includes an ALU that allows the difference to be calculated between any stop event and the start event, or between any pair of stop events, in the same or different channels. The PLL is contained on the chip, although external circuitry is needed for the core voltage regulation.



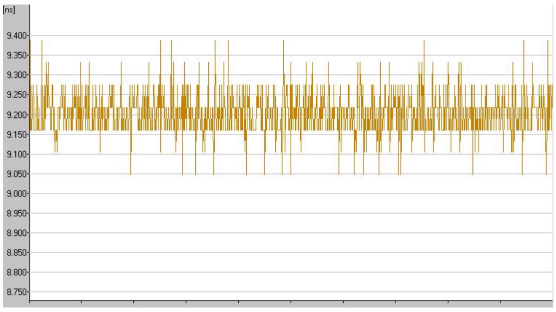
TDC-GP1 timing diagram

Note that a stop pulse received within 3ns of the start pulse will be ignored. Hence for operation in a TDOA system a fixed delay must be placed in one channel to ensure that this condition is not violated. Alternatively an externally generated start signal can be applied and the detector signals applied to the two stop inputs. In either case, care is needed to prevent lock-up if a pulse is detected in one channel and not the other. In the high resolution mode only one channel is available, but with twice the resolution (i.e. 125ps nominal).

The F1 includes a number of modes and facilities that are specific to the particle physics environment for which it was developed, and are of less interest in the ESM application. At its simplest, the F1 can be regarded as a higher resolution, multi-channel TDC.

ACAM market an evaluation system for the TDC chips that is suitable for laboratory field tests. It consists of a motherboard that can accommodate either one or two plug-in modules each having a TDC-GP1, or one module with a TDC-F1. The motherboard connects via a cable to a PC interface card, either PCI or ISA bus formats. Windows based software is supplied for control of the TDCs and collection of results.

When exercised using a laboratory pulse generator, rms errors of better than 100ps were obtained, showing that the device is capable of the precision needed for TDOA.



Typical TDC measurement

Simulation results

A simulation has been produced of a two antenna TDOA system. The antennas are assumed to be omni-directional and the antenna baseline is user specified. The following parameters of the receiver are user defined:

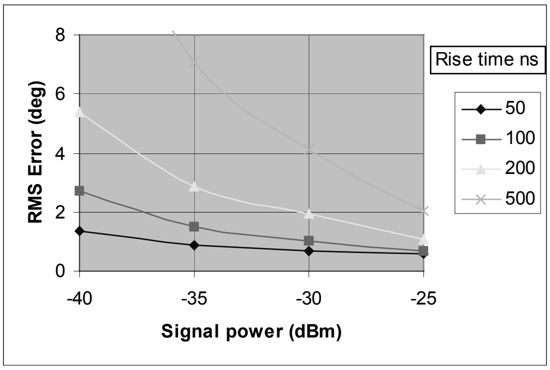
- RF noise figure (dB)
- RF bandwidth (GHz)
- RF gain (dB)
- Detector sensitivity (V/W)
- Detector impedance (Ω)
- Video noise figure (dB)
- Video bandwidth (MHz)
- Video gain (dB)

A mismatch between the two receiver channels can also be specified for the following parameters:

- RF gain (dB)
- Video gain (dB)

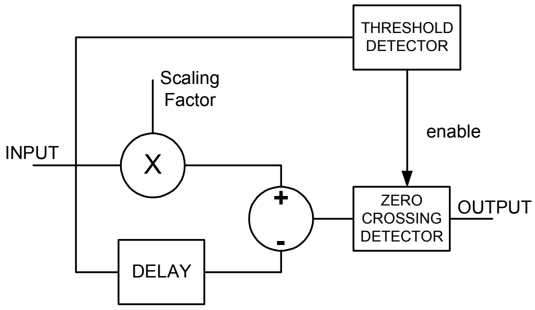
- Video bandwidth (%)

One or two signal sources may be specified, at arbitrary directions of arrival relative to the antenna baseline. The signals have trapezoidal pulse envelopes with user specified duration, rise times and fall times. Simulation results with varying pulse rise time and RF power level were in good agreement with theory.



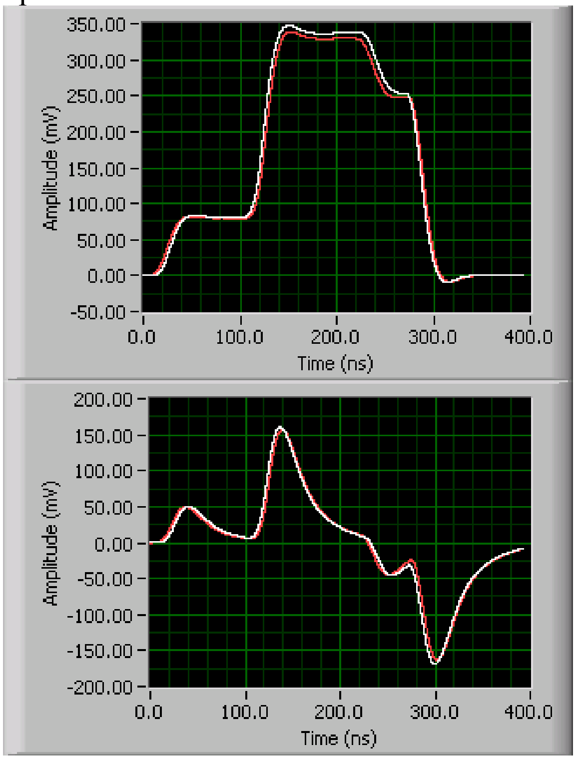
Rise time and RF power dependence

One area of concern is the effect of gain mismatch between the channels. Simulation showed that that a 0.1dB mismatch gave an offset of up to 3° in the bearing measurement. If it is not possible to match the channels (or remove the error by calibration), a constant fraction discriminator (CFD) may be employed, although this has the disadvantage of degrading the SNR. A CFD was incorporated in the simulation and shown to have the desired effect.



Constant fraction discriminator

Clearly a system relying on pulse leading edges will be unable to measure overlapping pulses, although the comparatively low sensitivity of the system, giving emitter mainlobe intercepts only, will reduce this problem. There is an option to include a high-pass filter before the thresholder, which will allow overlapping pulse discrimination, but again at the expense of SNR degradation. The decision whether to use this will depend on the operational environment.



Overlapping pulses, with and without high pass filter

Future Work

In the next year, it is planned to design and build a technical demonstrator, and perform trials against real radar systems. The demonstrator will be built around the ACAM TDC evaluation system, and will make maximum use of COTS components to minimise risk. Initial trials will make use of ESL's waterfront location to perform DF against marine band radars on an opportunistic basis. Subsequently it is proposed to perform more extensive trials against a wider variety of radar systems and in a higher pulse density environment.

References

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3. Wu J, Shi Z and Wang I, *Firmware only implementation of time-to-digital converter (TDC) in field programmable gate array (FPGA)* IEEE NSS 2003