# Passivation and High Temperature Effects of AlGaN/GaN HFETs

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## Abstract

*We report the behaviour of AlGaN/GaN HFETs from 20ºC to 600ºC. Key performance indicators such as maximum drain current, transconductance and pinch-off current are investigated as a function of temperature. The devices were found to be stable when subjected to continuous stress at 500ºC, which confirms the potential of GaN for high temperature applications. However, a severe degradation in $g_m$ is observed for one micron gate lengths. Post processed devices were also passivated with $Si_3N_4$ using different deposition conditions to determine its effect on the gate leakage current and breakdown voltage and identify optimum processing conditions in order to minimize current collapse at high frequencies.*

*Keywords: AlGaN/GaN HFETs, High Temperature, $Si_3N_4$ Passivation*

## I. Introduction

In recent years, the inherent advantages of wide bandgap semiconductors for applications in power electronic devices have driven a strong research interest in the GaN material system. The large bandgap of GaN (3.4 eV) compared to Si (1.1 eV) and GaAs (1.4 eV), results in higher breakdown fields, which are beneficial for high power operation, without intrinsic carrier conductivity difficulties becoming important until temperatures beyond 900K are reached [1]. Much attention is focused on AlGaN/GaN heterostructures for field-effect transistors, due to the high sheet densities and excellent electron transport properties associated with the induced two-dimensional electron gas (2DEG). Recent results has been impressive, with output power densities of 11.7 W//mm at 10 GHz reported [2]. In contrast, a power density of 1 W/mm at 10 GHz is currently considered the state-of-the-art performance for GaAs based power pHEMTs.

In this work, we present two critical issues in the performance of AlGaN/GaN power HFETs. The first concerns the degradation of key parameters such as the maximum drain current, ($I_d$), transconductance ($g_m$) and leakage current with increasing temperature. The second relates to $Si_3N_4$ passivation of post-processed HFETs. AlGaN/GaN HFETs suffers from 'current collapse', which translates into reduce output power at RF compared to DC. However, this effect can be mitigated by using $Si_3N_4$ passivation, but is also accompanied by a detrimental rise in the leakage current. Therefore, it is crucial that the passivation process is optimized. For this study, different $Si_3N_4$ deposition conditions were used and the changes in the gate leakage current and breakdown voltage investigated.

## II. Experimental Details

The device structure consists of a 30 nm thick AlGaN layer $Al_{0.26}Ga_{0.74}N$ and a 1.2 µm thick GaN buffer grown on a sapphire substrate. The HFETs were fabricated using a conventional route of mesa isolation, ohmic metallisation and gate metallisation (Fig. 1). The isolation mesa was etched to a

depth of 250nm and the ohmic contacts consist of Ti/Al/Ti/Au and the gate contacts formed using Ni/Au. $Si_3N_4$ dielectric films (~ 50 nm thick) were then deposited on post-processed HFETs in a commercial plasma enhanced chemical vapour deposition (PECVD) system. High temperature measurements were conducted in a furnace under flowing $N_2$ ambient.

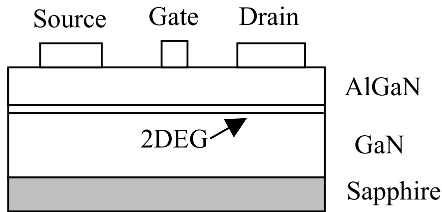


Fig. 1. Schematic device structure of AlGaN/GaN HFET.

## III. Results and Discussion

The HFET room temperature saturation current is close to 700 mA/mm and $g_m$ of 160 mS/mm obtained for a 1.0 x 75 µm gate device. Fig. 2(a) illustrates the typical transfer characteristics at room temperature and Fig. 2(b) depicts the 600ºC operation, the temperature at which the *I-V* curves remain stable.

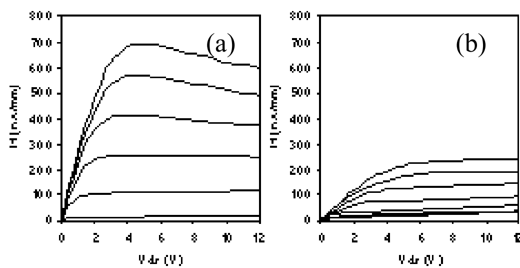


Fig. 2. Unpassivated AlGaN/GaN HFET *I-V* characteristics at (a) 25ºC and (b) 600ºC. $V_g$ = +1V, 0V… -7V in both cases.

Fig. 3 describes the gradual transition of $I_{d-max}$ and $g_m$ with temperature. $I_{d-max}$ is seen to reduce at a rate of 7.9 $mAmm^{-1}$/10ºC from 692 $mAmm^{-1}$ to 235 $mAmm^{-1}$ between 20ºC to 600ºC. Correspondingly, $g_m$ decreases at a rate of 1.9 $mSmm^{-1}$/10ºC from 161 mS/mm to 52 mS/mm for the same temperature range. $g_m$ reduces due to the reduction in channel mobility, $\mu$, resulting from an increase in polar optical phonon scattering with temperature. For sub-micron gates the channel transport is determined by saturation velocity rather than $\mu$, which may have a different temperature dependence. Future work on sub-micron gates will address this aspect.

When operated at 620ºC, the devices failed and gate burnout is typically observed. In a separate experiment, a device was continuously stressed at 500ºC for 15 minutes and cooled back down to room temperature. The original current level and pinch-off voltage are fully recoverable. However, repeating the same experiment at 600ºC resulted in either catastrophic failure or irreversible degradation to the devices. The failure of the contacts indicates the need for in-depth investigation of metal/semiconductor contacts to provide stability for the devices at elevated temperature.

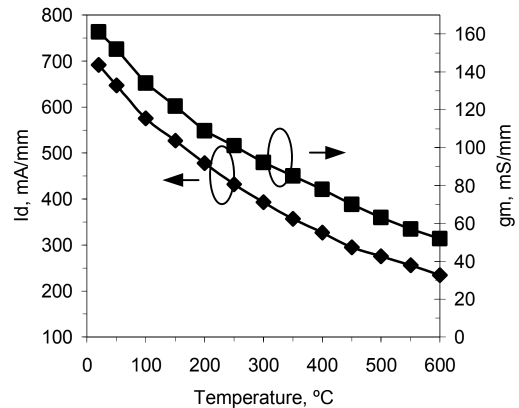


Fig. 3. Temperature dependencies of AlGaN/GaN HFET saturation current and transconductance.

the device to pinch-off. Fig. 4 illustrates the variation in the pinch-off current ($I_{d-pinch}$) with temperature and an increase of almost 5 orders of magnitude in $I_{d-pinch}$ is observed between 20ºC and 600ºC. The increase in $I_{d-pinch}$ at elevated temperatures is due to increased gate leakage current and also conduction in the GaN buffer. This

condition must be addressed since it may have adverse effects on noise sensitive applications and the stability of the devices.

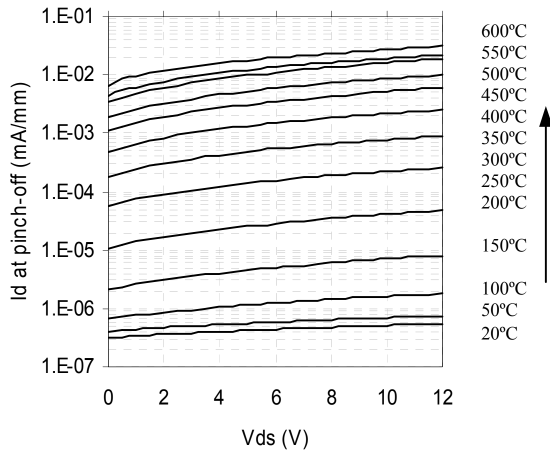


Fig. 4. Pinch-off drain current (at Vgs = -6V) plotted as a function of temperature.

Next, $Si_3N_4$ dielectric films were deposited on post-processed HFETs under different deposition conditions, such as variation in the substrate temperature, deposition pressure, RF excitation power and different $NH_3$ flow rates. The standard $Si_3N_4$ deposition conditions are set at 300ºC substrate temperature, 900 mTorr pressure, 25 W RF power and 5 sccm $NH_3$ flow rate. The devices were tested before and after passivation using both two and three terminal measurements.

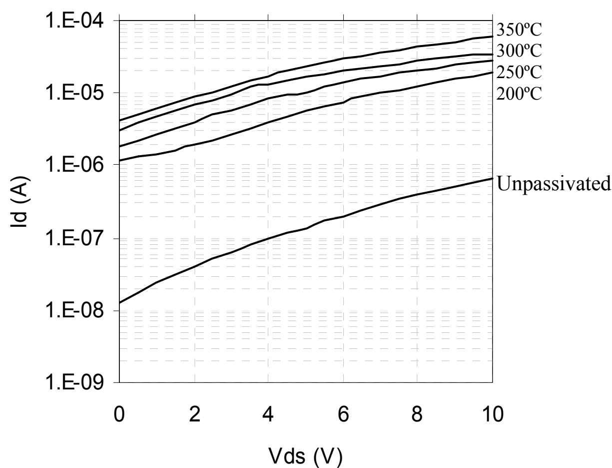


Fig. 5. Pinch-off drain current (at Vgs = -6V) of SiN passivated devices plotted as a function of substrate deposition temperature.

From Fig. 5, it can clearly be seen that reducing the substrate deposition temperature lead to reduced leakage currents. This suggests that higher deposition temperature may be indirectly damaging the device surface. The leakage also rose when deposited at 100W, but reducing the power to 6W also caused the leakage to rise. The former may be due to more energetic plasma bombardment at higher powers whilst the latter resulted from prolonged plasma exposure due to slow growth rates at this power. No significant change (from those obtained under standard conditions) is observed by varying the deposition pressure from 500 mTorr to 900 mTorr.

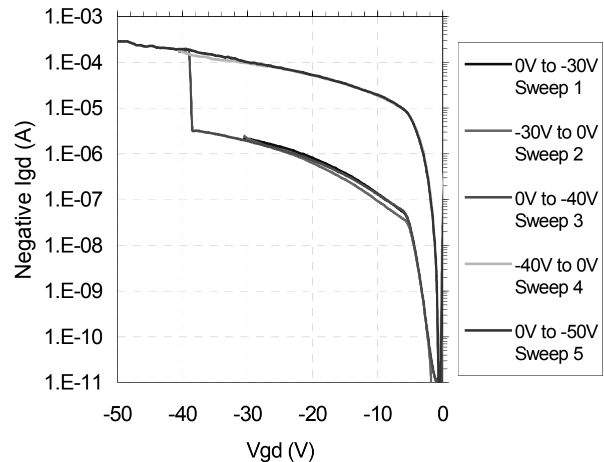


Fig. 6. An example of soft-breakdown on a $Si_3N_4$ passivated device (standard conditions), based on two terminal gate-drain leakage current. The device has a 1µm gate length, with 2 gate fingers, 70µm each.

An interesting observation is the occurrence of soft breakdown in the devices. From Fig. 6, a permanent degradation has occurred to the device at -38V bias (sweep 3). It is currently unclear whether this is a function of surface cleaning before gate deposition, gate edge profile, defects in the AlGaN or surface passivation. However, using a high refractive index $SiN_x$ (achieved by reducing $NH_3$ flow rate) seem to alleviate this problem, which may imply that a surface modification effect is responsible. This

phenomenon is still under investigation and will be detailed in future communication.
We have also investigated the effect of dielectric stress on the piezoelectric polarization charges of AlGaN/GaN HFETs. Previous reports in the literature offered conflicting and inconsistent results. $Si_3N_4$ films with different magnitude (tensile and compressive) of stress were deposited and changes in the maximum drain current studied. The induced dielectric stress was found not to be an issue in affecting polarization charges of the AlGaN/GaN structure. In addition, the use of dual-frequency PECVD should be treated with caution, since the low frequency component is found to induce severe ion bombardment damage to the AlGaN surface, which causes non-reversible degradation in the sheet charge and mobility.

## IV. Future Directions and Summary

This work is primarily concentrated in the development of GaN-based HFETs for high power/temperature applications. We have demonstrated operational devices at 600ºC and this clearly establishes HFETs as a viable candidate for high temperature applications. The next step will be to understand the physics behind the degradation mechanism of these devices at high temperatures. Gated and Linear Transmission Line Modelling will be used to isolate the changes in the resistances of the device with temperature. This enables us to separate out the low field temperature dependent transport of different parts of the device, such as the channel resistance, gap resistance and ohmic contact resistance.

The degradation (or burnout) of the device at temperatures higher than 500ºC is likely through the Schottky gate contacts. Therefore, alternative gate metals such as Pt or Pd can be examined. The reliability of the ohmic contacts after thermal cycling will also be addressed.

In summary, the high temperature robustness of AlGaN/GaN HFETs appears promising and a greatly enhanced knowledge resulting from this work will help in future device design and processing. Preliminary results for the $Si_3N_4$ passivation are encouraging and ongoing efforts are being directed towards optimising device performance in terms of gate leakage, current collapse and breakdown voltage.

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