

MMIC FREQUENCY DIVIDERS

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ABSTRACT

The maturity of transistor technology at millimeter-wave frequencies has increased interest in the design of high performance MMIC frequency dividers. This project aims to provide an active parametric frequency divider using PHEMTs. The objective is to achieve higher conversion efficiencies and easier cascading for higher order division ratios. This paper gives an overview of the subject area and outlines the proposed research idea and a brief description of work completed so far.

Keywords: MMIC frequency dividers, parametric PHEMT dividers, nonlinear subharmonic generation

INTRODUCTION

Frequency division is used in a variety of different systems from communications to electronic warfare (EW) systems. Rapid development of monolithic microwave integrated circuits (MMIC) technology is driven by the need for cheaper, lightweight and more compact devices with improved reliability, performance and lower power consumption. Hence the growing requirement for integration of frequency dividers.

Frequency division is a frequency conversion process similar to heterodyning. The absolute bandwidth is preserved in heterodyning, whereas in frequency division each frequency component in the input band is divided by a constant amount and thus it preserves the fractional bandwidth. Frequency dividers therefore have bandwidth compression capabilities.

This project aims to develop circuit configurations in MMIC form for an active parametric frequency divider. Once

designed, fabricated and tested, the performance will be evaluated and compared with theoretical predictions and also other major types of dividers e.g. regenerative frequency dividers. This research project is still in its early stages and is expected to be finished by 2006.

APPLICATIONS OF FREQUENCY DIVIDERS

Frequency dividers find applications in many different systems from low-cost theft prevention systems [1] to military applications. They are also essential to a variety of communications system needs. Some common uses are in conventional phase-locked loops and frequency translation or as prescalers in frequency counters and digital frequency discriminators. Additional applications lie in the area of EW, where the ability of the divider to compress bandwidth can be exploited in the processing of wideband signals.

The use of frequency division to down-convert microwave signals allows extremely wide-bandwidths to be reduced in frequency while retaining accurate frequency and phase information. Once in the lower frequency region, digital logic can be used to analyze and manipulate the signals for various application e.g. to produce coherent jamming signals to counter frequency agile, Doppler or coded waveforms [2].

TYPES OF FREQUENCY DIVIDERS

There has been a number of different microwave frequency divider concepts described in the literature. Each of these individual concepts may be categorized into two basic categories: digital and analogue. Digital frequency dividers yield instantaneous frequency division of a given signal on a cycle-by-cycle basis [3]. They are capable of broadband performances up into the microwave frequency range (up to 40 GHz). However due to the limitations of semiconductor device speeds, the digital frequency divider is difficult to realise without excessive power consumption (several watts DC power) at millimetre wavelengths.

Analogue dividers feature lower power consumption, simpler circuit designs and higher operating frequencies, which makes them attractive for communications purposes.

Two well-known analogue solutions are regenerative and parametric dividers. The regenerative divider was first described by Miller in 1939 [4]. Several papers on the theory of operation of regenerative dividers [4-6], as well as their noise performance [7-10] have already been reported.

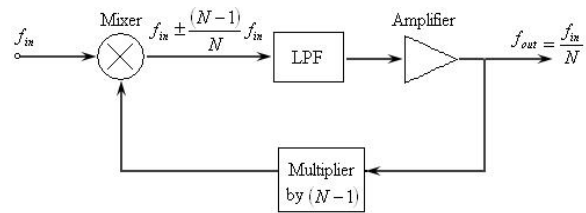


Figure 1 – Block diagram for regenerative frequency division by N

Figure 1 shows a block diagram of regenerative frequency divider. It consists of a mixer, low-pass filter and an amplifier in the forward path and a frequency multiplier in the feedback path. In brief the basic operation of this frequency divider is based on three conditions [6]: 1) a finite amplitude noise signal must be present in the loop, in order to provide an initial condition for regeneration, 2) the small-signal loop gain must exceed unity, 3) loop gain must be less than unity in the absence of an injected signal to avoid spurious oscillations [3].

Analogue regenerative frequency dividers are a good choice in order to simultaneously achieve very high operating frequencies, low phase-noise and low power consumption. However, their drawback is the synchronisation bandwidth [11], which is generally restricted to less than 20% [12-15].

Parametric frequency dividers [1, 16-18], however, often represent an optimum choice because of their broader synchronisation bandwidth and simpler circuit configuration, but need much more input power and achieve lower conversion gain [11]. Parametric division is to some extent a less common process, in which a subharmonic oscillation is generated from a nonlinear element. The most common element used in these dividers is a varactor i.e. the nonlinear capacitance of an abrupt junction diode. The basic theory of device operation is presented in [19] and [20]. Divider designs based on the empirical techniques are described in [1, 21-24]. Figure 2 shows a general diagram of a

parametric frequency divider. When properly adjusted, the circuit produces a response having a period which is an integral multiple of the excitation period.

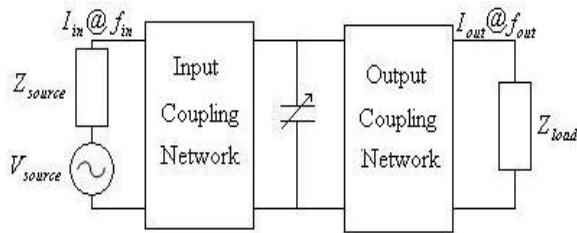


Figure 2 – General block diagram of parametric frequency divider

When generating subharmonics of the driving frequency, these circuits behave much like oscillators. As the output current builds up, nonlinear effects reduce the rate of amplitude rise and finally a steady-state with a constant output power is reached [24].

Although original divider proposals [4] had conceived the idea of a general division by N ($N \geq 2$), dividers subsequently designed and studied have been mainly divide by 2 configurations. To obtain greater division ratios frequency dividers have been cascaded, thus increasing amount of hardware and hence the need for more amplification. The approach we propose will eliminate this problem by using active devices in the design.

PARAMETRIC PHEMT DIVIDER

The principles of a nonlinear reactance frequency divider can be used and applied to an active semiconductor device such as a Pseudomorphic High Electron Mobility Transistor (PHEMT). The input nonlinear junction capacitance in a PHEMT is used with similar input and output matching networks to generate subharmonics, while amplification is achieved by the device transconductance.

The semi-unilateral property of active devices provides excellent isolation

between resonant input and output loops. It means that the output will not necessarily see the same impedance as the input. This implies that in order for frequency division to take place, all the input and output matching circuitry has to be on the input side of the PHEMT (Figure 3). So the required subharmonic current is generated in the input side and amplified by the controlled current source. A highly selective bandpass filter at the output selects the required output subharmonic frequency. So the output signal is amplified as well as divided in frequency.

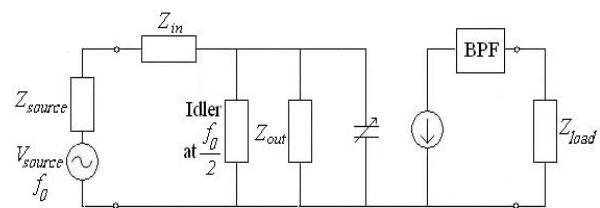


Figure 3 – Proposed diagram of parametric PHEMT frequency divider

To obtain higher order 2^N division we can cascade several dividers. This can increase the conversion efficiency but also increases complexity. This is well suited for fabrication using MMIC technology which enables complex circuits to be developed in a cheap way, in particular for large-scale production.

The associated gain of the nonlinearity used to achieve frequency division, compensates for most of the conversion losses. This fact enables more frequency dividers to be cascaded without worrying too much about signal degradation and power loss.

SIMULATION AND DESIGN

By nature, frequency dividers are potentially unstable, and since monolithic realisations do not allow for tuning, the ability to predict the overall circuit behaviour and performances by computer simulation is of prime interest [25].

Time-domain simulation is the more natural solution to study analogue frequency dividers because it allows direct analyses, even though it does not match all requirements for microwave integrated circuits design. MMIC designers are much more familiar with harmonic balance (HB) technique, as simulations in the frequency domain avoid many of the problems experienced when using traditional time-domain simulators to determine steady-state behaviour of analogue and microwave circuits [26]. But this technique is unable to spontaneously generate the subharmonic frequency which appears in frequency division.

For this project due to these limitations of HB analysis with frequency divider simulations, time-domain simulations are used initially. However for the eventual MMIC implementation of the circuit, HB analysis will be used. The software being used is Advanced Design Systems (ADS) from Agilent and AWR's Microwave Office.

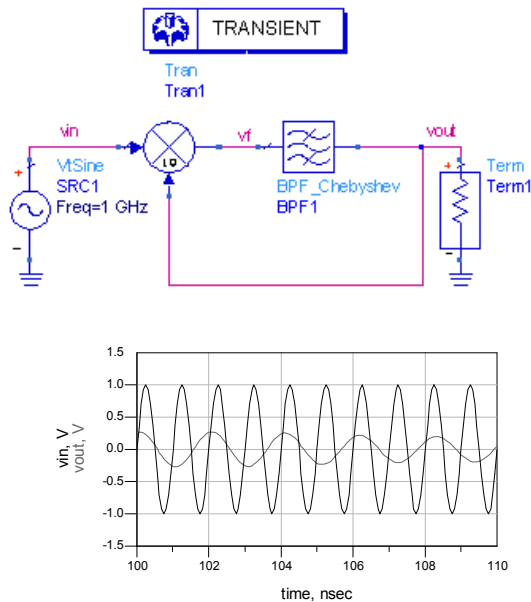


Figure 4 – Circuit diagram and simulation results showing a regenerative frequency divider

One of the project's initial aims is to model and simulate different types of frequency divider circuits in ADS such as regenerative, injection-locked and varactor frequency dividers. Figures 4 and 5 show divider schematics and simulation results for general regenerative and injection-locked frequency dividers respectively.

Since the PHEMT divider uses the principles of nonlinear reactance subharmonic generation, more time has been spent on understanding and modelling a varactor frequency divider circuit, in particular to correctly model the nonlinear capacitance.

A capacitor is defined as being a component whose charge is a function of voltage. Its capacitance is defined as the derivative of charge with respect to voltage,

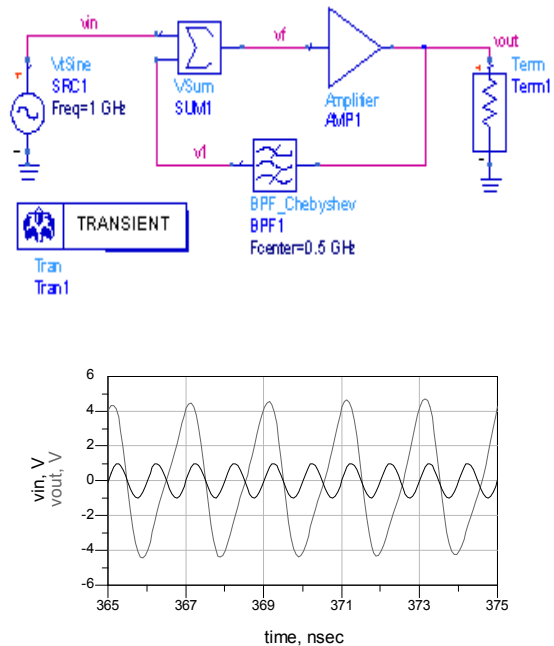


Figure 5 – Circuit diagram and simulation results showing an injection-locked frequency divider

$$C(v) = \frac{dq(v)}{dv} \quad (1)$$

The current through a capacitor is simply the time-derivative of the charge,

$$i(t) = \frac{dq(v(t))}{dt} \quad (2)$$

This can be expanded to

$$i(t) = \frac{dq(v(t))}{dv(t)} \frac{dv(t)}{dt} = C(v(t)) \frac{dv(t)}{dt} \quad (3)$$

A common mistake is to formulate the model for a nonlinear capacitor by starting with the model of a linear capacitor. If a capacitor is linear its charge is

$$q(v) = Cv \quad (4)$$

and so the current through the capacitor is

$$i(t) = \frac{d(Cv(t))}{dt} \quad (5)$$

Modelling the nonlinear capacitor by replacing C with $C(v)$ in (5) is not accurate and it will be problematic if used in simulators as it leads to charge not being conserved [27]. Thus using

$$i(t) = \frac{d[C(v(t))v(t)]}{dt} \quad (6)$$

produces large errors if C is a strong function of v and v varies significantly with t . Hence using Equation (2) to construct a model results in a model that is both accurate and computationally efficient. It suffers neither charge conservation problems nor accuracy problems common to equation (3) and (6).

The nonlinear voltage-dependent capacitor is modelled using a Symbolically Defined Device (SDD) inside ADS. The capacitor is replaced by a two port SDD whose current is defined in (2). For the parametric frequency divider, using an abrupt junction varactor, the diode's voltage-dependent junction capacitance is given by

$$C(v) = \frac{C_{j0}}{\sqrt{1 - \frac{v}{\Phi}}} \quad (7)$$

where C_{j0} is the zero-voltage junction capacitance, v is the instantaneous voltage across the varactor and Φ is junction's in-built potential.

This varactor model is inserted into a parametric frequency divider circuit as shown in Figure 6.

This circuit produces frequency division with appropriate circuit adjustments and settings. This work is being continued to determine better and more optimised solutions. In particular to optimise the transient simulator options to best match the output requirements. This will lead into a stronger and better starting point for the PHEMT frequency divider which will be tackled next.

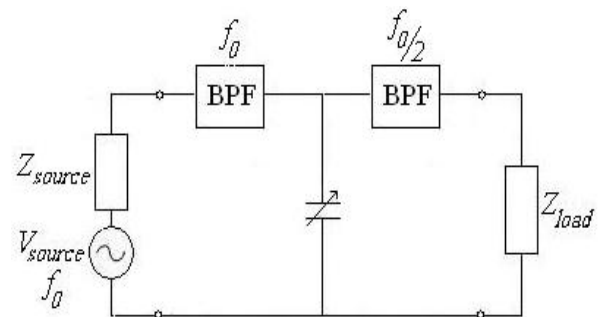


Figure 6 – Simple parametric varactor frequency divider circuit

CONCLUSIONS

An account of the proposed active parametric frequency divider using PHEMTs has been made and an overview of frequency dividers in general has been presented. Also a brief description of work completed so far has been given.

ACKNOWLEDGEMENTS

The authors would like to thank the Electro-Magnetic Remote Sensing (EMRS) Defence Technology Centre (DTC) for funding this research project.

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