Photonic Components for Analogue to Digital Converters

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Abstract

We investigate photonic component improvements necessary to realise wideband, high-dynamic-range analogue to digital (ADC) conversion, using optical signal processing techniques for interleaving or multiplexing a number of conventional electronic ADCs. We focus in particular on the laser and electro-optical modulator used for sampling the RF signal. In this paper, we present a preliminary study that uses a directly modulated optical link model to investigate the effects of laser jitter and modulator non-linearity on the performance of a photonic ADC.

Keywords: Analogue to digital conversion, microwave receiver, optical signal processing, photonic sampling, wavelength division multiplexing

Introduction

Wideband analogue to digital conversion is a critical problem encountered in communications, electronic warfare (EW) and radar systems [1]. Digital signal processing (DSP) in these systems has led to exceptional performance improvements and adaptivity, however the use of DSP in wideband systems has been restricted due to the difficulty in digitising the wideband signal.

Conventional electronic ADCs (EADCs) can operate reliably up to sampling rates of several 100's of mega samples per second (MSPS), with resolution exceeding 8 bits. The resolution drops below 6 bits for sample rates of several giga samples per second (GSPS).

ADCs using superconducting technology have been able to achieve high sampling rates, but the cryogenic (usually liquid helium or nitrogen) requirements may make it impractical for many systems applications.
Real world signals that need to be accurately measured and processed, such as those typically encountered in EW and radar applications, are usually non-repetitive. This rules out the use of sampling oscilloscopes, which only provide information about the average signal behaviour. In order to directly sample and process analogue signals in frequency ranges of tens of gigahertz, multi-bit ADCs that can sample at tens of gigahertz are required.

One or more of the following characteristics limits the performance of EADCs:

1. Sampling clock jitter
2. Sample-and-hold circuit settling time
3. Comparator ambiguity
4. Thermal noise

Thermal noise dominates the performance in high-resolution low-bandwidth systems while sampling jitter and comparator ambiguity limits high-sampling rates. The sample-and-hold circuit settling time determines the width of the sampling window, which in turn limits the RF bandwidth of EADCs. The ability to generate very short optical pulses means that this is the main EADC limitation that can be most significantly overcome using the PADC architecture.

Photonic ADC (PADC) architectures have been rigorously investigated in the past several years and demonstrator systems have been implemented [2-6]. By using photonics to interleave or multiplex a number of conventional EADCs (or also by using time spreading [4]), it is possible to get around the bandwidth limitations of the EADCs, set by the settling time of the input sample-and-hold circuits.

A schematic diagram of a generic PADC is shown in Figure 1. A high speed (8-bit) EADC might have a sampling gate width of 500 ps, which limits its bandwidth to a few GHz, even if a number of EADC circuits are electrically interleaved. However, optical sampling pulses can be much shorter than 500 ps, and can also have much higher repetition rates than electrical pulses. These advantages of optical sources can be used in a PADC to extend the bandwidth of the interleaved EADCs without compromising the resolution.

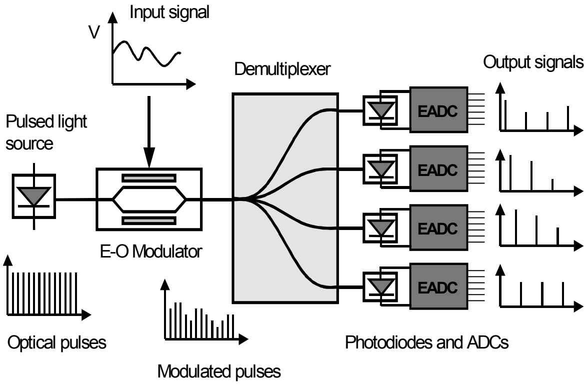

Figure 1. Schematic PADC architecture.

In this paper, we focus on understanding the advantages of PADCs compared to state-of-the art EADCs, and how to improve the performance of PADCs for both high bandwidth and high dynamic range applications. The analysis applies to different PADC architectures, including both time domain multiplexing (TDM) and wavelength division multiplexing (WDM). However, in this programme, we concentrate, in particular, on which improvements to components would be most beneficial to the development of high performance PADCs for EW and radar applications.

We use directly modulated optical link models to analyse the effects of laser noise and modulator non-linearity on the performance of PADCs. This route has been taken in order to identify the components that limit PADC performance. The analysis also quantifies the level of component improvement necessary to achieve a specified bandwidth and resolution (dynamic range).

The models used to analyse the PADC are discussed, followed by results from the modelling. We also discuss the development of a semiconductor electro-optic modulator, which can be applied to PADCs.

Photonic Link Model

An externally-modulated direct-detection model was used to investigate the bandwidth and dynamic range limitations of the RF optical link. The basic structure of the model is shown in Figure 2. Three standard approaches to the RF photonic link were implemented. The Bessel Function approach [7], a spreadsheet based model, and a model based on Fourier analysis were implemented. At the time of writing, these models use a continuous wave (CW) laser as the optical source. The modelling of effects of laser pulsing and optical cross-talk in components is in progress.

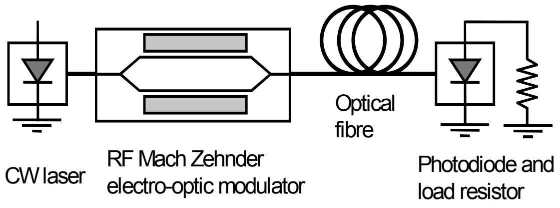

Figure 2. Single channel RF electro-optic link model.

Effect of Modulator Non-Linearity

The transfer function of the Mach-Zehnder (MZ) electro-optic modulator is inherently non-linear. However, by operating the modulator at quadrature, the region of maximum linearity can be used. The effect of this non-linearity is shown in Figure 3.

The dynamic range has been converted into an effective number of bits (ENOB) and plotted against the RF link bandwidth for different modulation depths and different numbers of parallel channels in a PADC. The lower set of lines are for a non-linearised modulator operated with a small modulation depth, set by the condition that the third harmonic spur is below the noise level. The upper set of lines are for a linearised device operated with a 50% modulation depth. The analysis shows that using a non-linearised modulator severely limits the PADC resolution for a practical system. On the other hand, if the modulator can be used up to 50% modulation depth, this puts high-resolution PADCs in a space that is currently beyond the capability of EADCs.

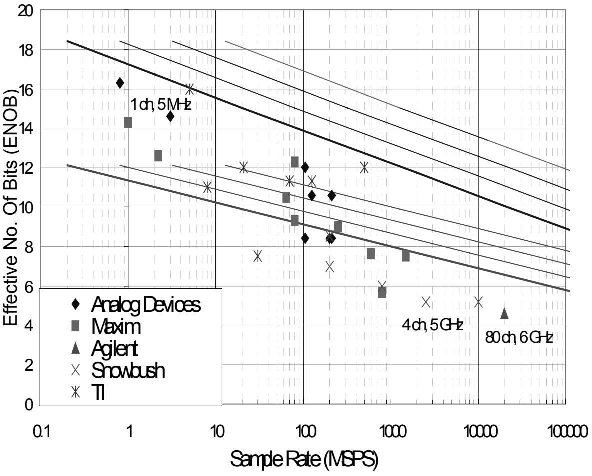

Figure 3. Results from the single channel RF link model plotted as the ENOB against sampling rate (assumed to be 2 x the maximum frequency to be measured). The lower lines are for 1, 4, 16 and 64 channel PADCs with conventional (non-linearised) modulators operating such that the third harmonic level is below the noise level. The upper lines are for 1, 4, 16 and 64 channel PADC's with a linearised modulator and a 50% maximum modulation depth. The symbols give the corresponding data for conventional EADCs, which can be interleaved in the PADC architectures.

Effect of Laser Jitter

In an EADC, the time and power jitter is defined as the tolerance that results in a digitising error of LSB/2 (LSB = Least Significant Bit). This definition has also been used for PADCs. If the laser pulses do not occur exactly when they should do, because of timing jitter, the signal will be sampled at the wrong time, and so the digitised output will differ from the signal voltage at the assumed (jitter free) sampling time. We use this definition to calculate the effect of jitter on the link dynamic range.

The jitter was modelled as a timing error of a single pulse from the optical source. This will give an indication of the most severe effects of timing jitter. The results of this **single sample** jitter are shown in Figure 4.

The maximum tolerable laser pulse timing jitter is plotted on the vertical axis against the sampling rate (assumed to be twice the maximum RF frequency to be sampled) on the horizontal axis for different ENOB values.

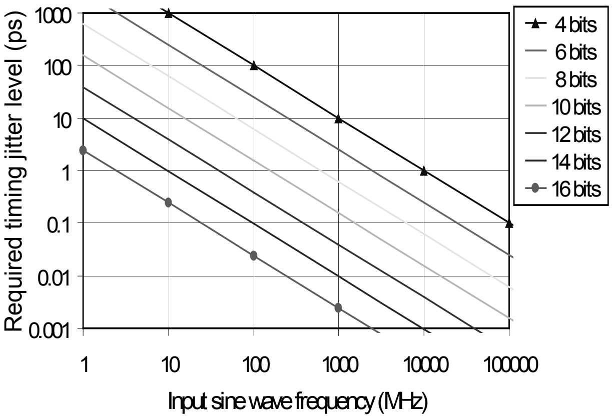

Figure 4. Graph showing the required **single sample** timing jitter limits plotted against the input sine wave frequency for different ENOB values.

Typical gain switched lasers have timing jitter levels of around 50 ps and power jitter levels of around 1% (although other techniques can be used to generate lower power jitter). It can be seen, from this single sample analysis, that to achieve the jitter requirements from a pulsed laser source may be a critical challenge for high dynamic range (>8 bit) systems, with input signal bandwidths approaching 10 GHz and beyond.

However, laser jitter is a fairly random phenomenon and its effect should be modelled as such. Also, in most EW and radar applications, the signal processing operations performed on the output digital values usually involve some form of averaging (an FFT, for example, to give the spectrum), which tends to reduce the effects of timing jitter in practice. Therefore, the effects of the jitter statistics were added to the model. So far, the parameters used for jitter statistics are somewhat arbitrary and its purpose is to demonstrate the modelling capability and the effect of using jitter statistics. As this programme progresses, the accuracy of the statistical model will be improved.

The time and power jitter values were assumed to be distributed normally, with a standard deviation of σ_t and σ_p respectively. The output of the Mach-Zehnder (MZ) modulator is Fast Fourier transformed (FFT), and the dynamic range is calculated as the difference in power level between the fundamental and the mean value of the noise floor arising from the jitter.

Calculations show that, for time jitter values of $\sigma_t = 1$ ps, a total of 1024 samples, and an RF input signal of 10 GHz, the average noise level is -92dB and the level of the fundamental signal is -38.6 dB, giving a dynamic range of 53.4 dB (8.6 ENOB). Similar calculations for $\sigma_t = 10$ fs gives a decreased average noise level of -132.5 dB, giving a dynamic range of 93.9 dB (15.3 ENOB).

The dynamic range as a function of time jitter and frequency is given in Figure 5. Compare this with Figure 4, where for a 10 GHz RF input, a 0.1 ps jitter level achieved 7 ENOB. Using jitter statistics in the model gives 12 ENOB at 10 GHz with 0.1 ps jitter.

A similar treatment is given to power jitter, which predicts that for single sample timing jitter, the pulse amplitude (for a 10 GHz signal) must be stable to 0.03% for an ENOB of 10, and 0.001% for an ENOB of 16. These numbers can be relaxed if the 1024 sample jitter approach is used to 1% and 0.02% respectively, if a linearised modulator is used with a 50% modulation depth.

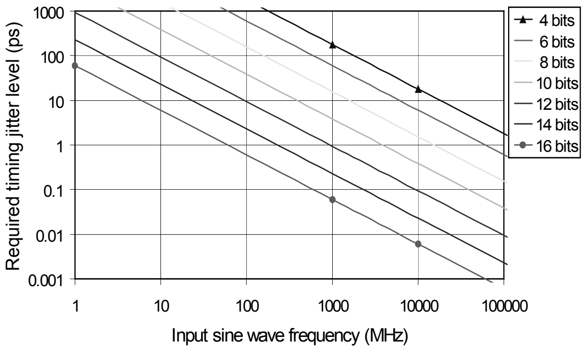

Figure 5. Graph showing the maximum **1024 sample** jitter limits plotted against the maximum frequency to be measured for different ENOB values.

Electro-Optic Modulator Development

The electro-optic modulator is a critical part in the PADC schemes under investigation and therefore, the improvements specific to PADCs have been included in the GaAs based wideband travelling-wave MZ modulator development programme at Filtronic.

The modulators are fabricated on 6-inch GaAs wafers and are based on Filtronic's high volume, high yield pHEMT process capability. RF packaging development and optical fibre attach use the pick and place capability of Filtronic Microtek Limited. We believe this approach is essential to achieve the very high performance components (such as linearised modulators, for example) required for PADCs, as well as for other military and commercial RF photonic applications.

Two optical waveguide approaches have been pursued in order to minimise the overall insertion loss of the devices. A 'thick core' waveguide design has been investigated with the aim of reducing fibre to waveguide coupling loss. A more standard 'thin core' structure has also been fabricated for low drive voltage devices.

The measured propagation loss of the optical waveguides fabricated is less than 0.25 dB/cm. The overall insertion losses (fibre-device-fibre) for thick core structures are less than 6 dB, while the thin core devices show about 8 dB of total loss, using lensed optical fibres. The main source of the extra loss in the thin core devices is the fibre to device coupling loss due to insufficient mode match between the coupling fibres and the optical waveguide.

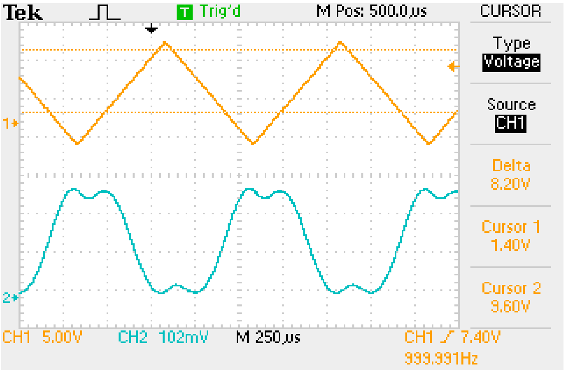

Figure 6. GaAs electro-optic waveguide Mach Zehnder modulator low frequency response (top trace: input voltage, bottom trace: output optical intensity).

The electro-optic response of a typical modulator is shown in Figure 6 for a low frequency triangle wave input voltage waveform. The switching voltage V_π is 8.2 V and the extinction ratio is >20 dB.

The **electrical** S-parameters S_{21} and S_{11} of the modulator RF travelling wave electrodes measured on wafer are shown in Figure 7.

The ability to fabricate on 6-inch substrates can enable cascaded MZ modulators, which can be used for photonic down-conversion. MZ arrays for commutator switch applications can also be investigated.

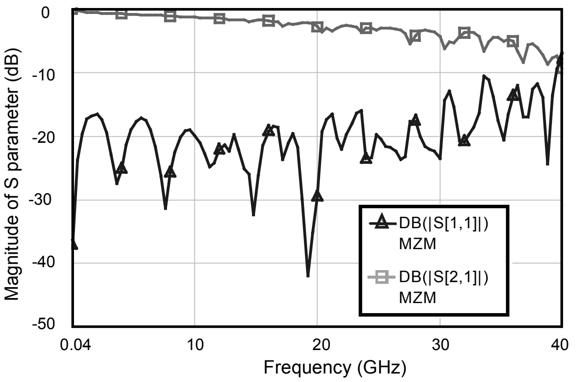

Figure 7. GaAs electro-optic waveguide Mach Zehnder modulator travelling wave electrode RF response (top trace: **electrical** S_{21} (RF loss), bottom trace: S_{11} (RF return loss)).

Discussion

The main reason for using optics in an ADC architecture is to overcome the bandwidth limitations of an EADC caused by the fixed width of the sampling gate, as optical sampling pulses can be much shorter than electrical pulses. The PADC samples the RF signal using optical pulses and then distributes these pulses to different electrical ADCs and the separation of the different pulses can either be by Wavelength Division Multiplexing or Time Division Multiplexing. The modelling shows that a PADC is most suited to extending the bandwidth beyond the range of current highest speed electronic ADCs, above 5 GHz. This is especially suitable for EW applications in which the total system needs to have a bandwidth of 20 GHz or more with 8 to 10 bit resolution. For this application, a linearised modulator is not strictly necessary, but would be advantageous. The pulse timing jitter for this application needs to be around 50 fs for 8 bit ENOB or 10 fs for 10 bit ENOB.

The modelling has focused on the possibility of using a PADC for radar applications - where the bandwidth might be only 100 MHz, centred around a known X-band frequency, but with a dynamic range of 95 dB (~16 ENOB). The model predicts that, to digitise a radar signal directly, without down-conversion, using a PADC with a conventional modulator, either the total number of channels would have to be extremely large (thousands), or IM3 spurii would compromise the SFDR. With a linearised modulator, however, this radar signal could be sampled directly, with a reasonable number of channels. This would require a timing jitter of around 5 fs (with 1024 sample averaging) and a power jitter of around 0.02%. This puts severe limitations on the pulse source. The total PADC sampling rate would have to be around 200 MS/s and the pulse width would have to be around 10 ps or shorter. Various approaches can be taken to reduce the pulsed laser timing jitter, although often at the expense of locking the repetition frequency to the round trip time of an external cavity, rather than the system clock frequency. Alternatively, an approach using electro-optic modulators to generate stable pulses could be used, as in some TDM architectures, but this usually requires quite complex circuits to generate the required mark-to-space ratio. This type of circuit, in particular, requires a very high yield modulator fabrication process.

An alternative approach to the radar application might be to down-convert the signal to base-band [7,8]. This could be achieved using an optical down-converter based on Mach Zehnder modulators. The sample rate would still be 200 MS/s, but the pulse width could be wider (around 1 ns or less – and still preferably < 100 ps). The timing jitter would be around 20 fs for single point sampling, or 500 fs for x 1024 averaging – the total averaging time however would be around 5000 ns which is much longer than a typical radar pulse. This performance cannot be achieved using EADCs because the sampling window needs to be longer to achieve the higher dynamic range – so the advantages of using photonics is still relevant.

Conclusions

In this preliminary study, we have analysed the performance of a generic Photonic ADC architecture based on interleaving or multiplexing conventional electronic ADCs. We have focused on the photonic component requirements for both wide-band (~10 bit) EW requirements and narrower band high-dynamic range (~16 bit) radar requirements. We conclude that the most promising application area for photonic ADCs with current electro-optic components is in EW receivers, where the wide bandwidth of photonics is particularly advantageous. However, by developing a modulator that is linear over a 50% modulation depth, our calculations show that photonic ADCs could have significant roles in digitising (down-converted) radar signals, even with dynamic ranges as high as 95 dB. For this application in particular, the jitter of a pulsed laser sampling source is a key issue.

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