

Hybrid Optoelectronics for Radar Signal Processing

V. Handerek and L. Laycock
BAE SYSTEMS Advanced Technology Centre
West Hanningfield Road, Great Baddow, Chelmsford, Essex CM2 8HN, UK

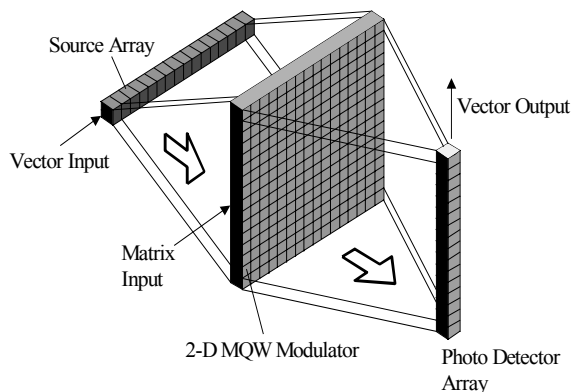
Abstract

This paper predicts that it is technically feasible to use analogue optical vector matrix multipliers as processors for signals with up to 90dB dynamic range. This can be accomplished by using algorithms similar to those for multiple-precision arithmetic in electronic processors. Various optical processor configurations can be anticipated. These extend from the basic analogue version offering 24dB dynamic range, where speed advantages of more than two orders of magnitude can be expected, through versions offering ~45dB dynamic range and speed advantages of about one order of magnitude, up to 90dB dynamic range configurations which should offer speed improvements of factors of a few times compared to state-of-art electronic digital signal processors.

Keywords: Optical vector matrix multipliers

Introduction

Recent telecommunications developments in fast (Gbit/s) laser arrays and multiple quantum well (MQW) modulators have spurred interest in one of the simpler yet more flexible and powerful optical processor architectures, namely the vector-matrix multiplier (VMM) [1]. A schematic view of such a device is shown below.



Schematic optical vector matrix multiplier

A set of numbers forming an input vector are represented as optical intensities by an array of sources. The light from each source is spread over a column of optical modulators, whose transmission represents the elements of a matrix multiplying the input vector. The individual products from each row of the matrix are collected and summed on a photodetector array to form an output vector. This particular configuration is optimised for very fast throughput at moderate accuracy. The major limitation of optics in the past has been that there is a restricted dynamic range. A recently announced processor product [2] operates with 8-bit digital precision, whereas it is widely quoted that dynamic ranges of 90 dB (30 bit precision) should be targeted by front-end processors for radar receivers. In order to maximise this processor's value to radar applications it would be very beneficial to be able to trade some of its vast speed for increased resolution through the use of suitable algorithms. This paper describes the outline of an approach to accomplish this.

Approaches for high precision and efficient computation

It is possible to use digital arithmetic logic processors of a given precision to operate with a larger number of significant digits through the use of multiple-precision algorithms. In fact, this is often used in conventional digital electronic processing. A similar approach may offer a solution allowing optical processors to be employed in situations requiring performance exceeding the basic precision of current equipment. The particular approach which is being considered for use with the vector-matrix multiplier is described below.

The basic architecture of an optical vector matrix multiplier was first proposed over a quarter of a century ago [1]. This processor represents numbers internally in a linear, analogue format, with external communication via standard binary digital inputs and outputs. Technological and fundamental physical limitations prevent the processor from providing exact correspondence with infinite accuracy between these digital and analogue number representations. However, exact correspondence can be expected up to a certain accuracy described by the number of reliable significant bits in the output from the processor. The arithmetic operations performed by the processor are multiplication and addition. In the general case, we may define a particular linear algebra processor which can be trusted to produce a reliable output with n significant bits. We can still use that processor for reliable linear computations with an integer multiple of the basic accuracy, $(r+1)n$ bits, if we break the calculation up into a set of subsidiary calculations, each of n bit accuracy. For the case of multiplying two scalar numbers, u and v , this can be done in the following way. We can break up the binary number u , which has $(r+1)n$ digits, into $r+1$ segments U_0, U_1, \dots, U_r , where U_0 represents the least significant n bits and U_r

represents the most significant n bits. Thus u is re-expressed as a polynomial in powers of 2^n :

$$u = \sum_{i=0}^{i=r} 2^{in} U_i$$

Similarly,

$$v = \sum_{j=0}^{j=r} 2^{jn} V_j$$

The product uv will then comprise $(r+1)^2$ sub-products, each weighted by the appropriate power of 2. Since the numbers are in binary format, the weighting is easily accomplished in the electronic domain merely by a shifting operation. $2r$ shifts are needed in total:

$$uv = \sum_{i=0}^{i=r} 2^{in} U_i \sum_{j=0}^{j=r} 2^{jn} V_j$$

Since u and v are both $(r+1)n$ digit numbers, the product uv has $2(r+1)n$ digits.

This approach was proposed for use with optical vector-matrix multipliers in the past [3]. For vector-matrix products, we need to extend the concept to take account of the effects of the dimensions of the matrices and vectors concerned. The discussion is here limited to products of vectors having M elements with square matrices of $M \times M$ elements. The product is therefore also a vector of length M , whose every element is calculated by the summation of M scalar products. The effect of this summation is to require a further increase in the accuracy required to fully express the value of the element. The additional number of binary digits required is $\log_2 M$ bits. The total number of bits d required to accurately specify the value of each element of the output from a vector matrix multiplier, where the input vector and matrix are specified to an accuracy of n bits, is therefore given by

$$d = 2n + \log_2 M$$

The implication of this argument is that the computation time will increase as the square of the number of segments into which numbers are divided for computation. This will not be true if a slightly more advanced algorithm is adopted. As the number of segments ($r+1$) is increased, the computation time T is predicted [4] to scale as

$$T \propto (r+1)^{\log_2 3}.$$

Technology advances for 8-bit optical processors

Most development effort for optical vector matrix processors has been aimed at producing units offering 8-bit digital precision at their outputs, given 8-bit precision values at their inputs. The main obstacles to achieving this have been the existence of losses in the optical systems, nonlinearity in the conversion from electronic to optical analogue signals, slow update speeds in spatial light modulators, and issues related to packaging. These problems most keenly affected the source and modulator components. Recently however, some major technical developments have occurred which have greatly improved prospects for commercialisation, since they directly impact all of the key problems experienced previously.

First of all, multiple-quantum-well devices have been successfully adopted for the optical modulation function. These devices have intrinsically fast response in the individual pixels (\sim GHz switching rates), low drive powers ($\sim 1\mu\text{W}/\text{pixel}$) and bias voltages ($\sim 5\text{V}$), and high contrast ratios ($\sim 100:1$). In itself, this technology represents a significant advance over previous liquid crystal spatial light modulator (SLM) devices, but more importantly, it is also compatible with the full range of standard process technologies

used for large scale component integration and hybridisation existing within the semiconductor industry. Thus large pixellated arrays of modulators can be constructed with photolithographic methods enabling very tight alignment tolerances and high fill-factors. Also, these arrays can be integrated with standard CMOS driver circuitry by 'flip-chip' mounting and solder bump attachment methods to provide compact hybrid assemblies [5]. Most recently, processing developments have allowed the production of arrays of 288×132 pixels with uniformity allowing accurate 8-bit grey-level resolution across the whole array [6].

For the sources, the main advance that has occurred is the development of vertical-cavity surface-emitting laser (VCSEL) arrays. These allow independent emitters to be used to generate the optical input vectors for the processor using direct modulation. This latter property simplifies the optical arrangement compared to external modulation and also allows much higher potential modulation rates (\sim GHz) for each source. The processing and hybridisation advantages discussed for the SLM case are also fully applicable to this new type of optical source.

Component technology for processors with greater than 8-bit precision

Close study of the literature on the key optoelectronic components used in emerging optical vector matrix processors suggests that it will be difficult to achieve analogue accuracy beyond the equivalent of 8 bits in the near future. Therefore, vector matrix multipliers accommodating greater dynamic ranges will have to rely on digital partitioning techniques for the foreseeable future. This approach is very compatible with component characteristics because it relaxes the analogue accuracy requirements on the source and modulator components, which have known difficulties, and exploits

the known strength of detector components, which normally offer excellent linearity and dynamic range. Also, in the case where the objective is to implement a fixed, mathematical transform on varying input data, the spatial light modulator would normally be used to represent the weight coefficients of the transform, and so would contain largely static data, while the optical sources would be used to represent the rapidly varying input signal. Once again in this case, the component properties offer a good match to the needs, since the SLM can normally only change its state much more slowly than the source array, due to the large quantity of data which needs to be fed to the SLM.

System performance predictions

This section presents predictions of processing speeds for analogue optical vector matrix processors intended for calculations requiring greater than 8-bit digital precision. The performance of current state-of-art electronic digital signal processors is quoted as 8 GMAC (Multiply-and-ACcumulate) operations per second, and this reference performance is used here for convenience.

The systems considered in this section all share the same spatial light modulator design, which is assumed to be 256 x 256 elements. The input and output vectors therefore each can comprise up to $V = 256$ elements, with each element being respectively represented using a laser or detector plus the associated signal

Conclusions

Comparison of the four groups of processors in the table leads to several conclusions. First of all, the dramatic speed advantage of the analogue processors is very clear. Any applications that do not require more than 24dB dynamic range can benefit from probably more than two orders

converter. The dynamic range R of the input values is directly linked to the external digital precision, according to

$$R = 10 \log 2^{(r+1)n}$$

Since digital partitioning requires that there be no loss of accuracy at the output, the value of n can be arbitrarily set between unity and up to no greater than half of the digital precision, d bits, of the analogue-to-digital converters used at the photodetectors. Once n has been chosen, the dimension M of each sub-matrix must then be set so that the accuracy of the output values is again not compromised, according to the expression for d given earlier. The number of sub-matrices which can be accommodated by the assumed size of the SLM is given by $(V/M)^2$ and the number each of sources and detectors which is needed to support fully parallel operation of these matrices is V/M times greater than for the analogue case. A 'slow-down' or delay factor compared to the analogue case was given above.

The table in Attachment I compares the computation speeds of some selected processors, relative to a state-of-art electronic digital signal processor delivering a 128-point complex discrete Fourier transform to 32-bit digital precision. All of the processors are assumed to use a 256 x 256 element spatial light modulator. The processors have been arranged into four groups, according to their different electronic hardware arrangements.

of magnitude reduction in processing times. Set beside the performance of the analogue processors, the speed benefits of the processors using digital partitioning are comparatively modest, but these configurations can still offer up to one order of magnitude speed improvement, depending on the dynamic range requirement and the degree of parallelism which is chosen.

References

[1] JW Goodman, AR Dias and LM Woody ‘Fully parallel, high-speed incoherent optical method for performing discrete Fourier transforms’ Optics Letters 2(1) (January 1978) p.1-3

[2] <http://www.lenslet.com/>

[3] CK Gary ‘Matrix-vector multiplication using digital partitioning for more accurate optical computing’ Applied Optics 31(29) (10th October 1992) p. 6205-6211

[4] DE Knuth ‘The art of computer programming Vol.2: Seminumerical

algorithms’ (2nd ed.) p. 278ff Addison-Wesley, London, 1981

[5] JA Trezza, JS Powell, C Garvin, K Kang and R Stack ‘Large format smart pixel arrays and their applications’ Proc. IEEE Aerospace Conf. 1998 p. 289-310

[6] U Arad, E Redmard, M Shamay, A Averboukh, S Levit and U Efron ‘Development of a large high-performance 2-D array of GaAs-AlGaAs multiple quantum-well modulators’ IEEE Photonic Tech. Letters 15(11) (November 2003) p. 1531-3

Option	Dynamic range <i>R</i> (dB)	External digital precision <i>(r+1)n</i> (bits)	Digital precision of input DAC <i>n</i> (bits)	Digital precision of output ADC <i>d</i> (bits)	Conversion rate (Msamples/sec)	Computation speed relative to electronic DSP	Required numbers of source, detector and converter arrays	Speed limiting component	Comments
A1	24	8	8	8	125	50	1	DAC	Emerging commercial product (analogue case) Components as above with digital partitioning
A2	48	16	3			2.8	64		
B1	24	8	8	8	500	200	1	DAC	Analogue processor 8 segment DP 8 segment DP
B2	72	24	3			7.4	64		
B3	90	30	4			7.4	256		
C1	45	15	5	15	80	5.3	8	ADC	3 segment DP 5 segment DP 6 segment DP
C2	90	30	6			2.5	64		
C3	90	30	5			1.9	8		
D1	45	15	5	14	125	8.3	16	ADC	3 segment DP 6 segment DP
D2	90	30	5			2.9	16		

Attachment 1 - Computation speeds for various optical vector matrix processor configurations using a 256 x 256 spatial light modulator to generate a 128-point complex discrete Fourier transform.