

Hybrid Optoelectronic Vector Matrix Processors for Radar Signal Processing

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Abstract

There will potentially be very large gains in computation speed and energy efficiency if a hybrid, digitally partitioned, opto-electronic vector matrix multiplier can replace state-of-art electronic processors for processing radar signals. Even at the likely maximum dynamic range of 90dB in the incoming radar signals, in the most attractive cases the hybrid processor can in principle provide between one and two orders of magnitude reduction in processing times. Power consumption per bit processed can also be improved using the hybrid approach.

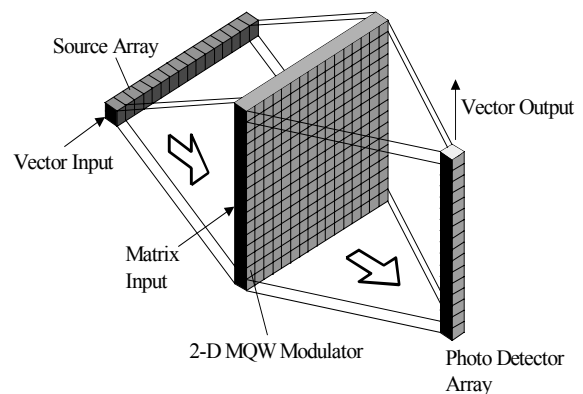
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Introduction

There is a need for faster processing hardware to provide modern radar systems with advanced capabilities such as real-time clutter removal and space-time adaptive beamforming (STAP) for jammer nulling. One approach which may help to meet this need may be to use analogue processing in parts of the signal processing chain. Analogue processing can offer extremely fast computation compared to digital electronic circuitry, but has the disadvantage that it traditionally suffers from limited or slow programmability, whereas electronic devices have relatively few programming limitations. In order to optimise both processing speed and programmability, it is attractive to consider the development of hybrid processors taking advantage of the best features of both approaches. The question then arises of how best to implement the analogue part of the signal processing chain. This paper considers the use of optoelectronic processors for this application.

Recent developments in fast (Gbit/s) laser arrays and multiple quantum-well spatial light modulators (MQW-SLM) have

spurred interest in one of the simpler, yet more flexible and powerful optical processor architectures, namely the vector-matrix multiplier (VMM) [1]. A schematic view of such a device is shown below.



Schematic optical vector matrix multiplier

This processor works in the following manner. A set of M numbers forming an input vector are represented as optical intensities by an array of sources. The light from each source is spread over a column of optical M modulators, whose transmission represents the elements of an $M \times M$ matrix multiplying the input vector. The individual products from each row of the matrix are

collected and summed on a photodetector array to form an output vector with M elements. This particular configuration is optimised for very fast throughput at moderate accuracy. The major limitation of optics in the past has been that there is a restricted dynamic range. A recently announced processor product [2] operates with 8-bit digital precision. Now, it is widely quoted that dynamic ranges of 90 dB should be targeted by front-end processors for radar receivers. Since it is signal voltages, and not powers, which must be represented at the front end of the processing chain, this requirement translates into a need to perform calculations with 15-bit precision. This need can in principle be met by trading some of the vector matrix processor's vast speed for increased resolution through the use of suitable algorithms [3-6]. One particular algorithm, known as a 'digital partitioning' approach, was the subject of an earlier part of the present work [4]. This paper examines some specific core radar processing tasks needing improved performance, and where digitally partitioned opto-electronic computation may offer useful benefits.

Choice of optical system for processor comparison

In order to compare the attractiveness of purely electronic and hybrid processors, we may use energy per bit and overall computation speed as relative yardsticks. While processing speed is important in all applications, energy per bit can be much less important in many applications, though this will need to be considered in, for example, airborne applications, as the size and weight of the processing hardware will be affected by this parameter.

While comparison of processing speed between hybrid and purely electronic processors is relatively easy, given assumptions about the overall frame rate,

vector dimensions and digital precision of the optical core processor, comparison of energy per bit is less easy as this depends on the performance of practical devices. The main devices in the analogue chain include digital-to-analogue converters, VCSEL drivers, the VCSELs themselves, the spatial light modulator, detectors, transimpedance amplifiers and finally analogue-to-digital converters at the output of the analogue subsystem. Examination of the performance of these devices shows that the main contributors to power consumption are the signal conversion circuits, VCSEL drivers and transimpedance amplifiers, whereas the power consumption of the MQW-SLM and its driver circuitry is likely to represent only a very small part of the total. The overall power dissipation of the VMM analogue processor is therefore expected to scale approximately linearly with the number of parallel optical sources and detectors used in the processor. In order to maximise the benefit of the optical approach, it is helpful to make this parallelism as large as possible. Also, in order to minimise the impact on processing speed of the digital partitioning approach, the digital precision of the output ADC should be as large as possible.

The choice of a notional configuration for a VMM was guided by all of the considerations discussed above. The resulting main parameters of the notional system were that the source and detector arrays should possess 256 elements each, with the detector array being read out at a rate of 100 M samples/s per vector element. (This rate is similar to that of the existing commercial system: 125M samples/s per vector element). In order to maintain accuracy in the digital partitioning algorithm, we require that output values should not be truncated. The digital precision allowed in the input vector is therefore restricted by that available for the output vector, together with the number of parallel sources. The total number of bits d required to accurately specify the value of

each element of the output vector, where the input vector of dimension M and matrix of $M \times M$ are both specified to an accuracy of n bits, is given by

$$d = 2n + \log_2 M$$

At the required processing rate, available components limit the digital precision of the ADC used after the detector chain to 14 bits. Allowing for the 256 parallel sources, the maximum allowable digital precision at the sources and the MQW-SLM was then 3 bits. The power dissipation of the system can then be expected to be similar to that of the commercial system (40W), with an allowance for the increased digital precision of the output vector, leading to a final estimate of a power consumption of 90W in the analogue subsystem.

Performance comparisons

The opto-electronic VMM described in the preceding section offers approximately 8 TMAC (Multiply and ACcumulate) operations per second. For comparison purposes, a nominal 'state-of-art' electronic processor offering 8 GMAC operations per second and consuming 4 W power was considered. Common 'front-end' radar processing tasks include Fast Fourier Transformation (FFT) and Finite Impulse Response (FIR) filtering. Correlation represents another area which is computationally demanding. The impact of a vector matrix processor on each of these tasks was considered separately.

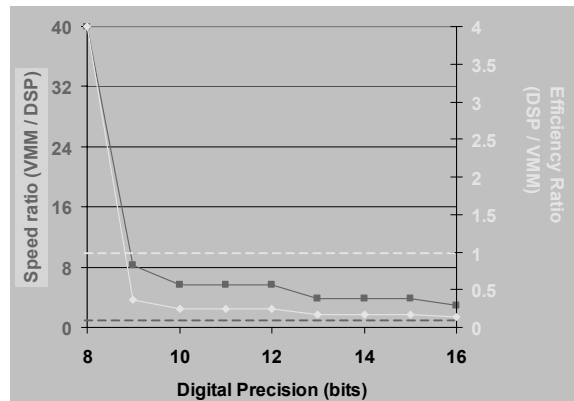
Fast Fourier Transformation:

The commercial opto-electronic VMM mentioned earlier is capable of performing a 128 point complex FFT operation to 8-bit accuracy in a single clock cycle. The processor configuration optimised for digital partitioning requires several clock cycles to achieve better digital precision, where each clock cycle is associated with a three-bit segment of the input numbers. As the digital precision of the input numbers is increased, more segments will be needed to

completely represent each number. If the input numbers are each divided into $(r + 1)$ segments, the computation time T is predicted [6] to scale as

$$T \propto (r + 1)^{\log_2 3}$$

The figure below shows the relative performance of the VMM compared to the electronic processor for 128 point complex FFT calculations as the digital precision of the computation is increased above 8 bits, up to the full 15 bits needed for the most demanding radar applications. The darker curve shows the variation of relative processing speed with digital precision, while the lighter curve shows the corresponding variation of energy consumed per bit processed. For the speed ratio, values greater than one indicate that the VMM is faster than the electronic processor. For the efficiency ratio, values greater than one indicate that the electronic processor consumes more power than the VMM. Dotted lines are added to emphasise the boundaries of improved performance for each feature.



Speed and power efficiency of VMM relative to floating-point DSP for FFT calculations

It is immediately clear from the figure that the basic analogue VMM offers dramatic speed and power efficiency advantages over the conventional electronic processor. With digital partitioning, the speed advantage is maintained to beyond 15 bits digital precision, where the VMM is still almost a factor of four times faster than the electronic processor. The energy consumed

by the VMM is, however, greater as soon as digital partitioning is used. This behaviour can be likened to a comparison between a sports car and a saloon; the sports car can reach its destination more quickly than the saloon, but consumes more fuel in the process!

Finite Impulse Response filtering:

FIR filters can be realised by either time or frequency domain methods. In the time domain approach, the output is given by:

$$y(n) = \sum_{m=0}^{M-1} x(m)h(n-m)$$

where M = number of taps on filter
 h = impulse response of filter
and $x(n)$ = sampled input signal values

If the input sequence has N samples of $x(n)$ to be processed, then each value of $y(n)$ requires $(M+N)M$ multiply-and-accumulate operations. The time domain approach offers a 'true' response, but imposes a large computation burden on the processor compared to the frequency domain method for long sequence lengths.

In the frequency domain approach, the output is given by:

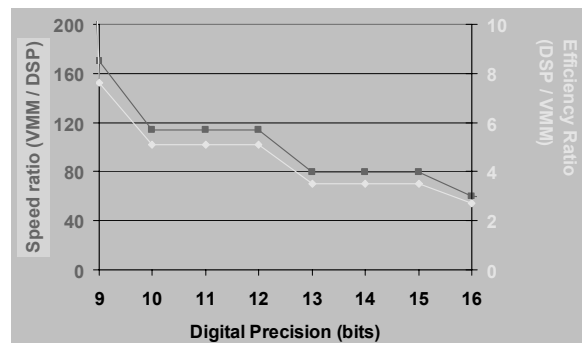
$$y(n) = F^{-1}\{F[x(n)] \bullet F[h(n)]\}$$

where F = Fourier transform
and other symbols are unchanged.

Frequency domain FIR filtering is normally computed using FFT algorithms for efficiency. For an impulse response and signal sequence length of L elements each, every value of $y(n)$ requires $(L \times \log_2 L + L)$ MAC operations. This leads to a relatively low computation effort for long sequences. The drawback of this approach is that distortions are produced because the calculation assumes that the signal is fully periodic beyond the sequence window. Also, the frequency domain method introduces processing delays which are discontinuous and prevent the filters from being used inside feedback loops [7]. Using

electronic processors, these drawbacks are usually accepted in order to shorten the processing time to an acceptable value. Because of the strong reliance on the use of FFT methods in the frequency domain approach, it is likely that the relative performance of an opto-electronic VMM would offer similar advantages to those already seen above. In addition, since the time domain approach is preferable if the processing resource requirements are not prohibitive, the VMM can provide much greater benefits.

The figure below shows predictions of the relative performance of the VMM compared to the electronic processor for time domain FIR filter calculations as the digital precision of the computation is increased from 9 to 16 bits. The conditions used for this comparison assume 1000 samples, 128 taps and 128 complex values for the impulse response. The darker curve shows the variation of relative processing speed with digital precision, while the lighter curve shows the corresponding relative variation of energy consumed per bit processed.



Speed and power efficiency of VMM relative to floating-point DSP for time domain FIR filter calculations

The figure clearly shows that in this case, both the speed and power consumption performance of the VMM provide strong benefits over the electronic processor across the full range up to 15 bits digital precision and beyond.

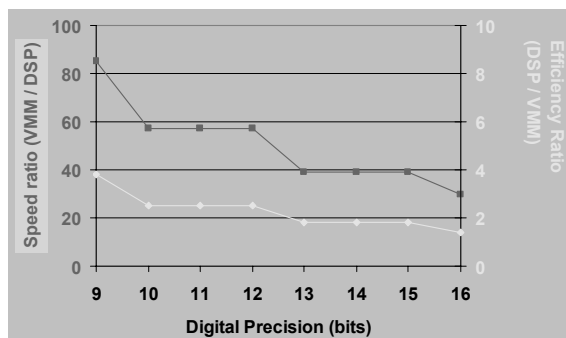
Correlation processing:

The cross-correlation coefficient C between two series, U and V , which might represent radar signal streams with n elements each, can be calculated based on the following expression [6]:

$$C = \frac{n \sum U_j V_j - \sum U_j \sum V_j}{\sqrt{(n \sum U_j^2 - (\sum U_j)^2)(n \sum V_j^2 - (\sum V_j)^2)}}$$

where all summations are taken over the range $j = 0$ to $j = (n-1)$.

Just as for the FIR filtering case, cross-correlation can be performed in a direct way by implementing the above formula or by using a shortcut approach in the frequency domain. If the latter approach is adopted, then the relative performance of the opto-electronic VMM and a purely electronic processor can be expected to be similar to that already seen for the case of fast Fourier transformation. The figure below shows performance gains which may be expected using the direct approach. These follow similar trends to those seen for the FIR filter case.



Speed and power efficiency of VMM relative to floating-point DSP for correlation calculations

Conclusions

There will potentially be very large gains in computation speed and energy efficiency if a hybrid, digitally partitioned, opto-electronic vector matrix multiplier can replace state-of-art electronic processors for processing radar signals. Three types of computation commonly needed in radar

signal processing were examined, taking into account the likely need to accommodate digital precision sufficient for 90dB dynamic range in the incoming radar signals. In all cases, the dramatic speed advantage of the opto-electronic analogue processor is very clear. Even at the maximum dynamic range, in the most attractive cases the hybrid processor can in principle provide between one and two orders of magnitude reduction in processing times. Power consumption per bit processed can also be improved using the hybrid approach. Current work is investigating some fundamental physical aspects of the opto-electronic system to determine the practicality of building a vector matrix multiplier specially adapted for digital partitioning.

References

- 1 Goodman, JW, Dias, AR, and Woody, LM, 1978, Optics Letters **2**, 1-3
- 2 <http://www.lenslet.com/>
- 3 Gary, CK, 1992, Applied Optics **31**, 6205-6211
- 4 Handerek, V, and Laycock, L, 2004, Proc. EMRS-DTC 1st Technical Conference, C18
- 5 Gibor, D, 2005, Proc. European Workshop on Photonic Signal Processing for Defence Applications, DP2
- 6 Knuth, DE, 1981, The art of computer programming Vol.2: Seminumerical algorithms (2nd ed.), p. 278ff, Addison-Wesley, London
- 7 Jeruchim, MC, Balaban, P, and Shanmugan, KS, Simulation of Communication Systems, p. 94ff, Plenum, London

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