# GaN-Based Heterojunction FET's on 100mm Si Substrates

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## Abstract

*The growth of AlGaN – GaN based heterojunction field effect transistor structures has been successfully demonstrated on 100mm diameter (111)Si substrates. Improvements in material quality have enabled uniform crack-free wafers to be realised with 2DEG properties comparable to material grown on sapphire and SiC. Both large area and 1μm gate length devices have been fabricated and the transistor DC characteristics assessed. Good mesa to mesa isolation, and transistor pinch-off is observed, whilst 1μm gate length devices show excellent high voltage properties with no breakdown observed up to -100V.*

Keywords: GaN, AlGaN, Si, HFET, HEMT

## Introduction

GaN-based RF devices have the potential to replace established GaAs technology in high power amplifiers by offering to deliver five times higher power at frequencies up to at least 40GHz. Furthermore, GaN devices have demonstrated comparable RF noise performance to GaAs devices but the superior breakdown field makes GaN ideally suited for a robust low noise amplifier. As large area insulating GaN substrates are unavailable, current GaN devices are produced on SiC substrates, which offer the best lattice match and thermal conductivity but are only available in diameters up to 75mm. As a scalable lower-cost alternative to SiC, GaN growth on Si substrates is being investigated which have the potential to scale to 150mm diameter, compatible with foundry production facilities.

Recently, major advances have been reported by groups working within the US, Japan and Europe, demonstrating the potential of GaN devices on SiC substrates. For example, Cree Inc. announced 38W continuous-wave (CW) power at 10GHz [1], Fujitsu reported 150W CW power at 2.1GHz and 54% power-added efficiency (PAE) [2], Daimler-Chrysler have demonstrated the first European GaN-based MMIC [3], and QinetiQ has demonstrated a 57W pulsed power module (10% duty cycle) with 32% PAE [4]. Furthermore, recent results reported in Europe show that the high frequency and noise performance of GaN devices on Si substrates is approaching that of GaN devices on SiC. A power density of 6.6W/mm at 2GHz [5] and 1.9W/mm at 10GHz [6] was demonstrated whilst a device with a unity current gain cut-off frequency ($f_T$) value as high as 46GHz, a maximum oscillation frequency ($f_{max}$) as high as 92GHz, and a noise figure (NF) of 1.1dB measured at 10GHz has also been reported [7].

The use of Si substrates readily available at 150mm diameters represents a key route to cost reduction in this technology and manufacturing advantage. However, growth of high quality GaN epitaxy on Si is significantly more difficult than growth on SiC due to the dissimilarity in crystal structure and thermal expansion properties of the materials which result in the formation of cracks in the epilayer that are detrimental to device performance. The formation of cracks can be mitigated by the inclusion of strain engineering layers during growth which enable the growth of thick (>2µm) (Al)GaN films on Si. We have previously reported a review of strain engineering techniques and described in detail growth experiments to study graded composition buffer layers on 50mm (111)Si [8].

In this article, which builds from the earlier work, we report advances in the MOVPE growth of GaN on Si and demonstrate HFET structures grown on 100mm (111)Si substrates with properties comparable to material grown on sapphire and SiC. Devices and test structures were fabricated and a summary of device DC characteristics is presented.

## MOVPE growth of GaN HFET's on 100mm (111)Si substrates

HFET structures were grown by MOVPE using a Thomas Swan CCS platform on high resistivity ($>10^4\Omega$cm) 100mm diameter (111)Si substrates. Details of the growth sequence were described previously [8]. We have found that an atomically flat oxide-free Si surface is important for successful epitaxy. To achieve this we use a standard RCA clean with a final HF step prior to loading into the MOVPE reactor followed by a brief high temperature anneal. The epilayer structure consists of a thin (~35nm) AlN seed layer followed by a graded $Al_xGa_{1-x}N$ buffer layer where x was graded from x=1 (AlN) to 0.05, followed by an insulating GaN layer. The total thickness of the layer stack was ~1.5µm. Finally, an undoped $Al_xGa_{1-x}N$ barrier layer (x=0.27) with nominal thickness 28nm was grown on top. Due to the band offset between GaN and AlGaN, a potential well is formed in the conduction band at the interface between the GaN buffer and the AlGaN barrier. A net dipole exists across the AlGaN due to large built-in polarisation fields. This dipole is balanced by mobile charge from carriers populating the potential well, surface states and acceptors within the GaN [9]. The carriers within the potential well form a two dimensional electron gas (2DEG) which acts as the channel of the device. A sheet carrier density, $N_S$ of $9\times10^{12}$cm$^{-2}$ was determined by mercury contact CV (capacitance – voltage) measurement, which is comparable to equivalent HFET structures grown on sapphire and SiC substrates. Fig. 1 is a contactless eddy current map of sheet resistivity for an HFET on a 100mm (111)Si substrate (5mm edge exclusion). The mean sheet resistivity is 483Ω/sq. with a standard deviation of 13Ω/sq. giving a uniformity figure of 2.7%.

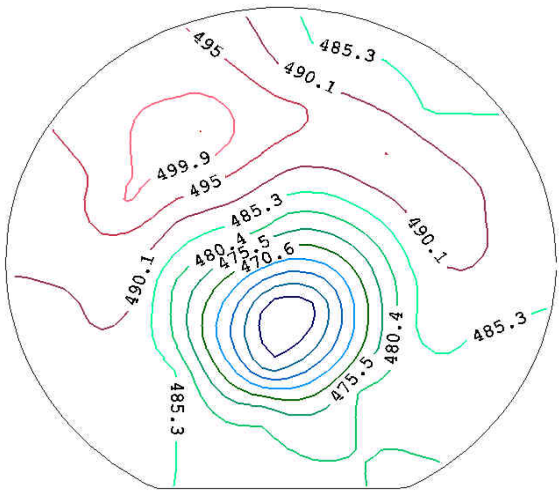



Figure 1. Lehighton sheet resistivity map of HFET on 100mm (111)Si substrate (5mm edge exclusion). The mean sheet resistivity is 483Ω/sq. with a standard deviation of 13Ω/sq. giving a uniformity figure of 2.7%.

## Device Fabrication and Assessment

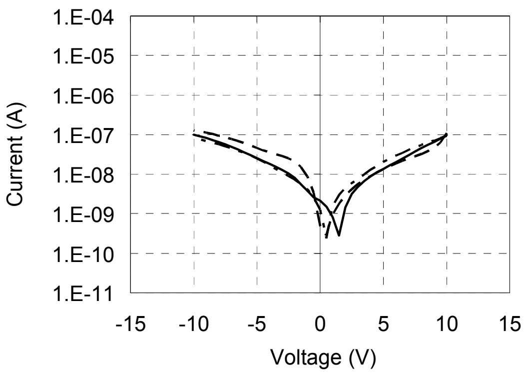
Device fabrication was undertaken on 33mm × 35mm rectangular samples sawn from the 100mm wafers. Device isolation was achieved by reactive ion etching of mesas to below the 2DEG. Ohmic contact metallisation was TiAlPtAu alloyed in rapid thermal annealer and Schottky gate contacts were NiAu. Below is a summary of measurements of test structures and device assessment before passivation.

*Ohmics/TLM*

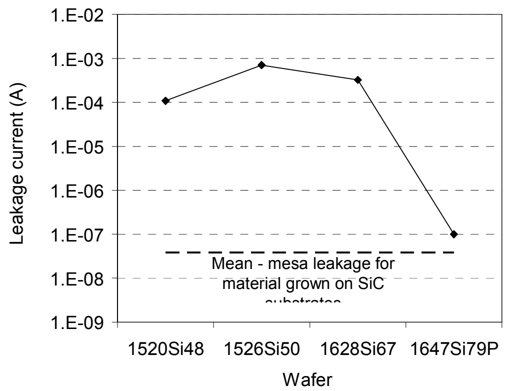
The IV (current – voltage) characteristics for TLM structures with nominal gap sizes of 5µm, 10µm, 15µm and 20µm were measured to determine the contact resistance ($R_C$). A mean $R_C$ of 1Ωmm was calculated.

*Mesa to mesa leakage*

The mesa to mesa leakage current was measured between two isolated mesas with Ohmic contacts (150µm × 100µm) 10µm apart between the 150µm sides, shown in Fig. 2(a). The leakage currents at 10V bias were 94nA, 96nA and 110nA, comparable to material grown on SiC. Fig. 2(b) compares the mesa to mesa isolation with that obtained for material grown on SiC and earlier growth on Si substrates.




(a).




(b).

Figure 2. Mesa to mesa leakage current; (a). between three test structures (150µm × 100µm, 10µm gap), sample 1647Si69P; (b). history of leakage current at 10V bias for GaN on (111)Si comparing current material (1647Si79) with previous material.

*Large area FET devices*

Large area devices ("FatFET's") with gate width of 150µm and length 100µm were fabricated as test structures. Characteristics were measured using a parameter analyser and an automated probing station. Fig.3 shows an overlay of CV profiles using an 18 point array. The mean capacitance was 44pF, equivalent to an AlGaN thickness of 27nm. The mean sheet carrier density was $6.5\times10^{12}cm^{-2}$.

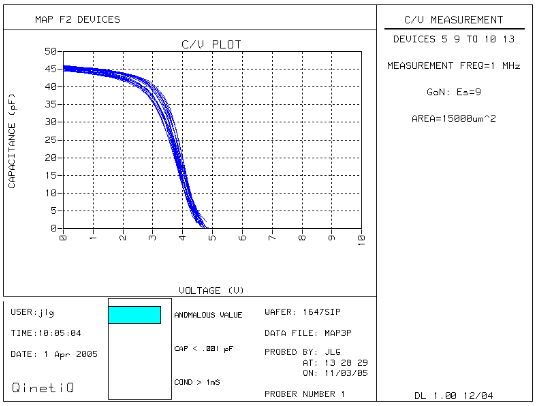
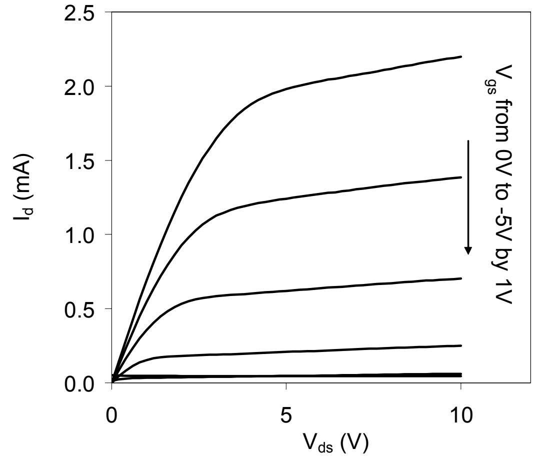
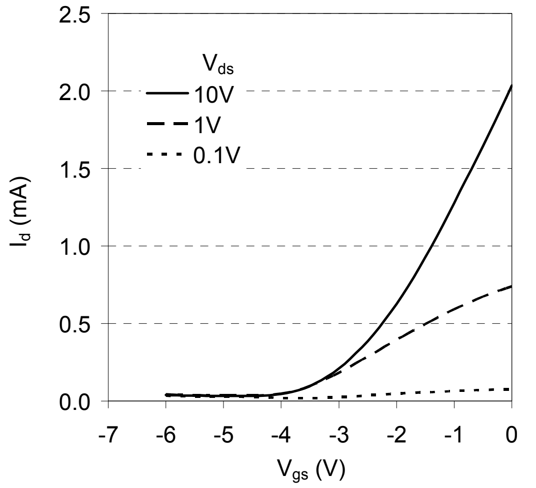



Figure 3. Overlay of CV profiles from FATFET (150µm × 100µm).

Transistor characteristics were mapped for FatFET devices. Fig. 4(a) is a typical output characteristic measured on an individual device up to a $V_{ds}$ of 10V, and Fig. 4(b) is the transfer characteristic for the same device. The drain current increases linearly with $V_{ds}$ below saturation, indicating that the source and drain contacts are Ohmic. In saturation, the characteristics have a slight positive gradient indicating a measurable output conductance, which would have an adverse effect on amplifier gain. For all the devices measured, a low level of drain current leakage is observed in pinch-off.




(a).




(b).

Figure 4. Typical transistor characteristics for a FatFET device; (a). Output characteristic for $V_{ds}$ up to 10V ($V_{gs}$ from 0V to -5V in steps of 1V); (b). Transfer characteristic for a $V_{ds}$ of 10V, 1V and 0.1V.

Fig. 5 shows a map of $I_{dss0}$ ($V_{ds}$=20V) which reveals a radial pattern with higher currents observed away from the centre of the wafer. The drift mobility extracted from the transistor characteristics (saturated region) for the majority of the devices in Fig 5 was ~750cm$^2$V$^{-1}$sec$^{-1}$. These values are slightly lower than typical values we obtain for comparable HFET structures grown on sapphire (1000cm$^2$V$^{-1}$sec$^{-1}$) and below the value of 1200cm$^2$V$^{-1}$sec$^{-1}$ typical of the same structure grown on SiC [10]. It is also lower than the figure implied by the $N_S$ determined by mercury contact CV and $R_S$ determined by contactless eddy current map which gives ($\mu=[N_S R_S q]^{-1}$) a mobility of just over 1400cm$^2$V$^{-1}$sec$^{-1}$. This discrepancy may have arisen due to degradation of the material during processing and is the subject of further study.

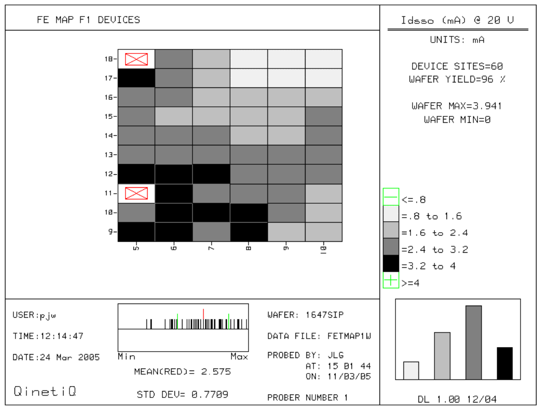
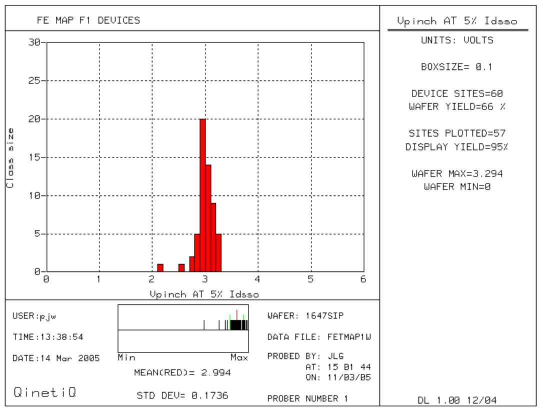
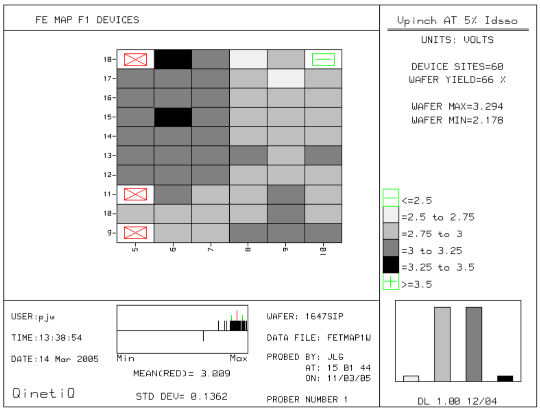



Figure 5. Map of $I_{dss0}$ at $V_{ds}$=20V. A radial pattern is revealed with higher currents observed away from the centre of the wafer.

A histogram and map of pinch-off voltage, $V_p$ for FatFET devices is shown in Fig. 6 (a) and (b) respectively. Setting the pinch off criterion to 5% $I_{dss0}$ produces a $V_p$ of 3V (0.17V standard deviation) and device yield of 95%. Reducing the pinch-off limit to 1% $I_{dss0}$ increases $V_p$ to 3.8V (0.1V standard deviation), but reduces the yield to 56%.




(a).




(b).

Figure 6. (a). Histogram and (b). map of pinch-off voltage, $V_p$ for FatFET's using a pinch-off criterion of 5% $I_{dss0}$. This gives a yield of 95% (60 device sites). The mean $V_p$ was 3V with 0.17V standard deviation.

*1μm gate length devices*

Devices with 1μm gate length were fabricated. The gate – drain reverse IV for three such devices is shown in Fig. 7. The voltage was swept from +2V to -100V. Good repeatability is obtained between devices with no indication of breakdown observed up to -100V, which is encouraging for high voltage operation.

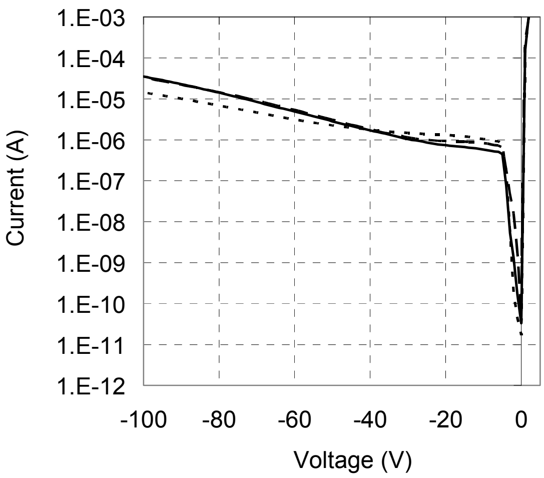



Figure 7. Gate – drain reverse IV for three 1μm × 50μm devices.

## Conclusions

The crack-free growth of GaN HFET structures on 100mm diameter (111)Si has been successfully demonstrated. Initial assessment has shown sheet carrier densities comparable to equivalent structures grown on SiC substrates and good cross wafer uniformities (2.7%) have been achieved, however, channel mobilities are lower than those obtained for comparable structures grown on SiC substrates. DC characterisitics of transistors exhibit good pinch-off, device to device isolation and reverse breakdown in excess of 100V. This is an important demonstration of the scalability of the GaN HFET process towards current GaAs foundry capabilities, which is a key objective of the programme.



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