X-band GaN Power Devices on Si Substrates

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Abstract

GaN HFETs offer the potential to dramatically improve the performance of solid-state microwave power amplifiers. Here we report on progress towards a low cost/manufacturable solution based on GaN growth on Si substrates. 0.25μm T-gate devices have been produced with f_t *up to 40GHz. The effect on power devices of the lower thermal conductivity of Si compared to the more normal SiC substrates has been simulated and it has been found that in general the power handling is reduced by about a factor of two.*

Keywords: GaN, AlGaN, Si, HFET, HEMT

Introduction

Recent developments in GaN-based RF FETs have demonstrated their potential to replace GaAs devices in high power amplifier applications. The superior breakdown field available in GaN devices means that they are able to deliver at least five times higher power compared to GaAs devices at frequencies up to 40GHz, with comparable RF noise performance.

Due to the high power densities demanded from GaN HFETs, self heating of devices is a significant issue. Therefore, due to its high thermal conductivity, the substrate of choice for GaN growth is SiC. However, although 100mm diameter SiC has very recently become available commercially, it will still be relatively expensive. Although Si has a lower thermal conductivity than SiC, the significantly lower cost of Si substrates and their availability in larger diameters makes them an attractive alternative for all except the highest power applications. In particular, the availability of Si wafers in sizes up to 150mm, and above, means that device wafers could be processed in existing foundry production facilities. GaN on Si therefore offers a scaleable technology which is potentially much cheaper compared to GaN on SiC substrates.

Rapid progress is taking place worldwide in the field of GaN microwave power devices. In Japan, high powers have been achieved for packaged devices using GaN on SiC substrates. Mitsubishi has demonstrated 140W at 5GHz (pulsed) [1], NEC achieved 230W CW at 2GHz [2], and Eudyna 100W at 2.8GHz [3]. However, the highest power from a single chip has been generated for a device in GaN on a silicon substrate. Nitronex reported in December 2005 that they have achieved 368W from a 36mm wide device for 1% duty cycle pulse operation at 2.14GHz (300μs pulses) with excellent drain efficiency of 70%. This dropped to a highly respectable 65W when measured cw[4]. These results have been achieved by a combination of improvements in epitaxial growth and by changes in device architecture through the use of techniques such as recessed gates and field plates.

In previous manuscripts [5,6] we have reported on issues relating to growth by MOVPE of GaN-based HFET structures on 100mm (111)Si substrates. These include the removal of the Si native oxide to allow epitaxial growth to take place and control of the tensile strain introduced by the large lattice and thermal expansion mismatches present between GaN and Si. By using strain engineering techniques we have been able to demonstrate GaN HFETs on Si substrates with sheet carrier densities, N_S, of 9×10^{12}cm^{-2} and mean sheet resistivities, R_s, of 483Ω/sq with a uniformity figure across a 100mm wafer of 2.7%. These results are comparable to the data measured for equivalent structures grown onto 50mm SiC substrates where the lattice and thermal expansion mismatches are significantly smaller. We have also previously reported the DC characteristics of device structures, showing good pinch-off and device to device isolation, and reverse breakdown voltages in excess of 100V.

In this article we report RF results from 0.25μm T-gate devices produced using QinetiQ epitaxy and, GaN on Si layers sourced externally. We also present simulations showing the effects of the lower thermal conductivity of Si substrates on the likely high power performance of devices.

Epilayer sources

GaN on Si material grown within this programme is produced by MOVPE [5]. Another popular growth technique for GaN on Si is Molecular Beam Epitaxy (MBE). We have procured and processed MBE GaN on 100mm (111)Si wafers from an external source. The general layer structures of the two types of material are similar, consisting of a strain accommodation layer deposited onto the Si substrate, followed by a relaxed GaN layer, with a thin AlGaN barrier layer. A 2-Dimensional Electron Gas (2DEG) forms at the GaN/AlGaN interface. In detail however, the two growth techniques do give layers with different structural characteristics. For example Figure 1 shows typical Atomic Force Microscopy (AFM images) of the surface of these two types of material. The MOVPE grown material consists of islands approx 20nm high and 20μm across compared to the MBE material which is again composed of islands 20nm high but in this case they are around 2μm across.

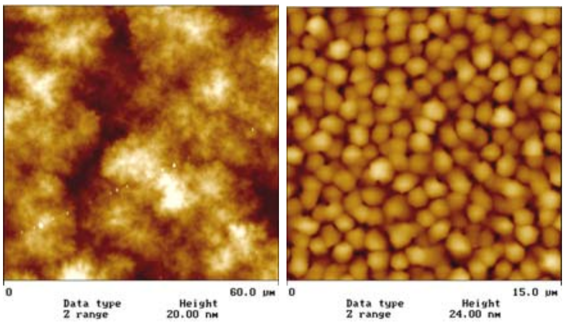

Figure 1. AFM images of a) MOVPE and b) MBE grown GaN HFET layers on Si.

Contact resistance (ohm.mm)	0.64±0.06
Rsheet	462±12
L_g (μm)	0.25
I_{dss0} (mA/mm)	720±50
G_m (mS/mm)	183±9
V_p(V)	-4.07±0.11
f_T (GHz) @ Vgs -3.25,Vds 20V	17-25
f_{MAX} (GHz) (2x125μm)	35-45

Table 1. HFET device results for GaN on Si HFETs.

HFET device processing

Small test transistors were fabricated using both material types with basically similar electrical results. There was close cooperation between Sheffield University and QinetiQ in the process development.

The measured DC and small signal RF data obtained from the best wafer is summarised in table 1. The cross-wafer uniformity is excellent and comparable to that obtained for the more conventional GaN on SiC processed at QinetiQ. Another wafer with somewhat shorter gate length as measured electrically, showed f_T of up to 40GHz.

Mesa to mesa isolation varied somewhat from wafer to wafer, but was adequate for DC purposes.

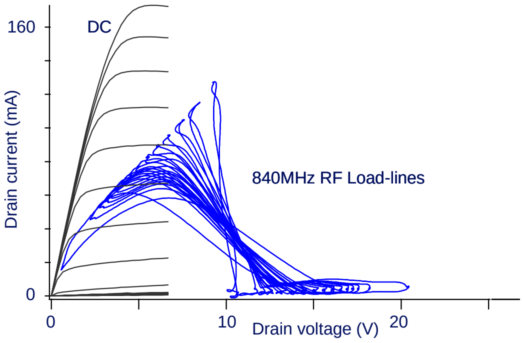

Figure 2. Load-lines for varying ouput load for a 2x125µm HFET. Vds=10V, class A.

Large Signal Measurements

So far the highest RF power output achieved is 1.8W at V_{ds}=30V and 2.8GHz from a 8x125µm 0.25µm gate length device. Comparable devices processed on GaN on SiC at QinetiQ give about 4W/mm for this bias condition. Lower than expected RF power is a common problem with GaN HFETs. In order to quantify the RF-DC dispersion of the devices, time-domain load pull measurements were carried out at Cardiff University. Figure 2 shows an example of how the RF loadline varies as the output impedance is varied. It can be seen that at RF, the output voltage swing is much smaller than the DC measurement and cannot access the low voltage, high current region. This is known as current-slump or knee-walkout and is usually ascribed to surface trapping. At present the same effect is seen on both internally and externally sourced GaN on Si material, and is worse than is seen for GaN on SiC devices. One very good feature which can be seen in the figure is that excellent pinch-off can be achieved at RF, which is essential for high efficiency operation.

RF Loss

One concern with GaN on Si substrates has been the RF loss in the substrate. We have measured the loss in a section of 50ohm co-planar waveguide on both GaN on Si and GaN on SiC. The results are shown in Figure 3 up to 50GHz. The loss for GaN on Si was about three times higher, but this is still not significant compared to the loss seen in circuits.

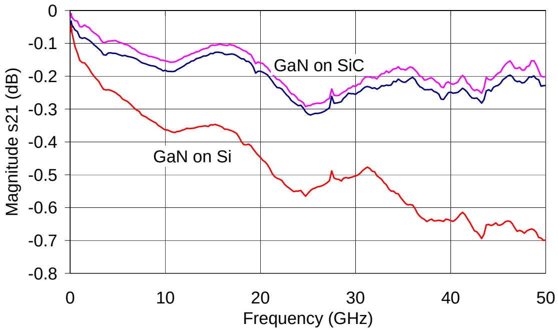

Figure 3. Loss in a 2mm section of 50Ω CPW line

Thermal effects in GaN on Si

The thermal conductivity of Si is up to a factor of 3 lower than that of SiC. It is therefore important to understand the likely consequences of this on power device performance. In order to examine these effects, we have carried out modelling of the thermal resistance of a range of different geometry multi-finger power transistors as a function of heat-sink temperature and input power. For small transistors, the use of Si substrates instead of SiC resulted in an approximate doubling of the thermal resistance and therefore a halving in the power handling capability of the transistors.

However, it was also found that for large power devices, with lateral dimensions that are significantly larger than the thickness of the semiconductor, the thermal resistance was dominated by the die attach and packaging materials. Figure 4 shows how thinning the silicon substrate and using a high thermal conductivity package (copper rather than copper-tungsten) gives a more significant benefit for an 8mm power cell, compared to the small two finger device.

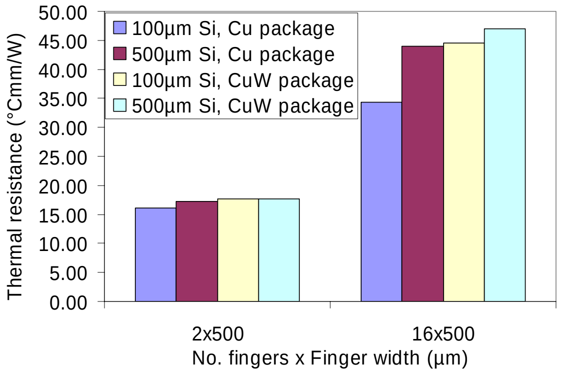

Figure 4. Thermal resistance of a large and small power transistor with thinned and unthinned Si substrate. Finger spacing 50µm, package thickness 1mm.

Conclusions

0.25µm T-gate transistors have been successfully fabricated in GaN grown by MOVPE and MBE onto 100mm Si substrates. These devices have been demonstrated to operate at frequencies suitable for X-band applications with a maximum f_T of up to 40GHz. However, poor DC-RF dispersion limits the maximum power output at this time to under 2W/mm. Improvements in material quality and device architecture should result in significant improvements.

Modelling of the likely effects of the lower thermal conductivity of Si substrates compared to SiC indicates that the use of Si results in a halving in power handling capability.

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