

## Optimisation of High Temperature Performance and Reliability of GaN HFETs

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### Abstract

*We report on the high temperature operation of GaN HFETs. Measurements and analyses of device characteristics at temperature from 25°C up to 500°C have been conducted on AlGaN/GaN HFETs on Si substrates. Good high temperature performance was demonstrated, and sub-micron gate length devices were found to have less temperature dependence at elevated temperature operation compared to >1µm gate length devices. A surface pre-treatment was also optimised for reproducible effectiveness of the Si<sub>3</sub>H<sub>4</sub> passivant.*

Keywords: Gallium nitride, heterostructure field effect transistors, high temperature operation, surface leakage.

### Introduction

AlGaN/GaN HEMTs on Si substrates have attracted considerable attention in recent years, with output power densities reaching 12 W/mm at 10 GHz [1]. Conventional sapphire substrates are low-cost but exhibit poor thermal conductivity and are available only in small sizes. SiC substrates have achieved the best AlGaN/GaN HEMT device performance to-date. However, their high costs are unattractive for commercialization. Si substrates are an attractive alternative since they are available in large size, are low cost and have good thermal conductivity compared to sapphire. GaN growth on Si substrates, however, is problematic due to the 56%

thermal expansion coefficient difference between the substrate and the epitaxial layer. The resulting large tensile strain build-up can cause cracking. A strong reduction in drain current density with increasing temperature has been observed in AlGaN/GaN HEMTs on sapphire and SiC substrates. Arulkumaran *et. al* [2] recorded a 76% fall in open channel current between 20°C and 350°C ( $L_g = 3 \mu\text{m}$ ), while Gaska *et. al* [3] reported only a 33% fall ( $L_g = 0.25 \mu\text{m}$ ), both on SiC substrates. There are no reports of the high temperature performance of HFETs on Si substrates.

Passivation (in the form of deposited Si<sub>3</sub>N<sub>4</sub>) of the surface of the device is essential to reduce the so-called 'current collapse' [4]

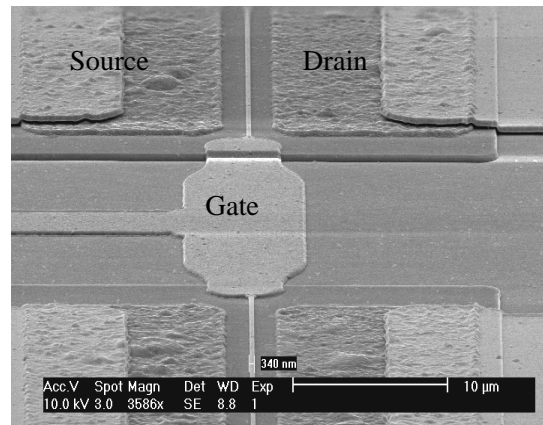
which causes an undesirable reduction in output current in conjunction with an increase in the knee voltage when operated at microwave frequencies. However, passivation can have mixed success due to contaminants on the HFET surface such as resist and oxide, which can cause problems with device reliability.

In this paper we report on the temperature dependent DC performance of AlGaIn/GaN HFETs grown on Si substrates and assess the influence of gate length (0.12  $\mu\text{m}$  to 100  $\mu\text{m}$ ) in order to gain a better insight into the controlling mechanisms. Also we demonstrate an improvement in the reproducibility of the passivation process by the optimisation of a surface pre-treatment.

### Experimental details

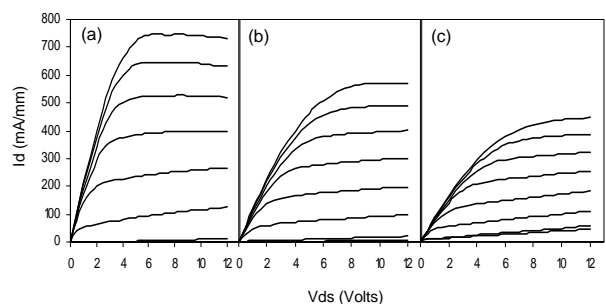
The AlGaIn/GaN layers were grown by QinetiQ using metal-organic vapour phase epitaxy (MOVPE) on 4-inch Si (111) >10 k $\Omega\text{cm}$  resistivity substrates. The device structure consists of a 1 $\mu\text{m}$  graded AlGaIn buffer layer, followed by an undoped 0.5 $\mu\text{m}$  thick GaN buffer and an undoped 28nm thick Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier. The mesa device isolation (200nm depth) was achieved using inductively coupled plasma etching. Thermally evaporated Ti/Al/Ti/Au (20/100/45/55 nm) metallization was used for the ohmic contacts, annealed at 850°C for 20 seconds under N<sub>2</sub> ambient. The sheet carrier density measured by capacitance-voltage was  $9 \times 10^{12} \text{ cm}^{-2}$ , and the room temperature drift mobility found to be  $950 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . The sheet resistance and contact resistance were determined from TLM measurements to be 600  $\Omega/\square$  and 1.3  $\Omega\text{mm}$ . The gate contact consisted of Ni/Au (20/200 nm), with contact lithography used for 1  $\mu\text{m}$  gate dimensions or larger and e-

beam lithography for 250 nm and 120 nm gate lengths. Ti/Au (20/300 nm) was used for bond pads and the devices were not passivated. High temperature measurements were conducted in a furnace under flowing N<sub>2</sub> ambient.



**Figure 1.** Section of a 350 nm gate AlGaIn/GaN HFET used in the high temperature measurements.

Figure 1 shows the typical layout of the devices used in the high temperature measurements. A novel leakage current test structure [5] was used to measure the surface and bulk leakage components separately as a function of temperature.



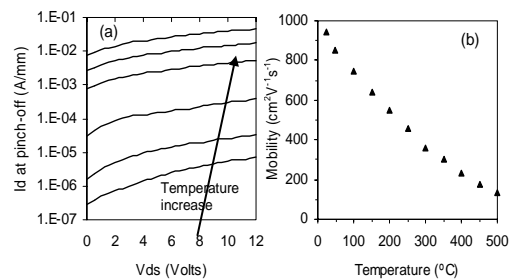
**Figure 2.** I-V characteristics for a 120 nm gate length HFET (gate width = 50  $\mu\text{m}$ ) at (a) 25°C, (b) 300°C and (c) 500°C. Gate potential was swept from +1V to -6V, in increments of -1V.

## Results and Discussion

Figure 2 shows the typical DC  $I$ - $V$  characteristics of an unpassivated 120nm gate length AlGaN/GaN/Si HEMT at three different temperatures. Excellent pinch-off characteristics with  $I_{dss0}$  of 650mA/mm and transconductance ( $g_m$ ) of 150 mS/mm obtained at 25°C. No short channel effects were observed, which indicates a high concentration of deep-levels in the GaN buffer [6]. The off-state breakdown was ~90V and the extrinsic unity gain cut-off frequency ( $f_t$ ) was 22 GHz as measured for a 0.25 $\mu$ m gate length device. Figure 2(b) and 2(c) shows the  $I$ - $V$  curves when operated at 300°C and 500°C, with  $I_{dss0}$  of ~480 mA/mm and 390mA/mm, and peak  $g_m$  of ~105 mA/mm and 75 mS/mm respectively. The  $I$ - $V$  curves remained stable and reproducible during high temperature operation. The increase in knee voltage with temperature increase is a result of the increased resistance along the ungated source and drain regions and the increase in output conductance is due to increased buffer leakage. Upon cooling to room temperature from 500°C, the original characteristics were restored, indicating no permanent degradation to the device.

A four orders of magnitude increase in drain leakage ( $I_d$  at pinch-off) was observed between 25°C and 500°C as is shown in Figure 3(a). This increase in drain leakage is comparable to results obtained from HFETs fabricated on sapphire and SiC substrates [7,8], which suggests that good isolation of the channel by the GaN buffer from the Si substrate was maintained even at 500°C. Figure 3(b) shows the

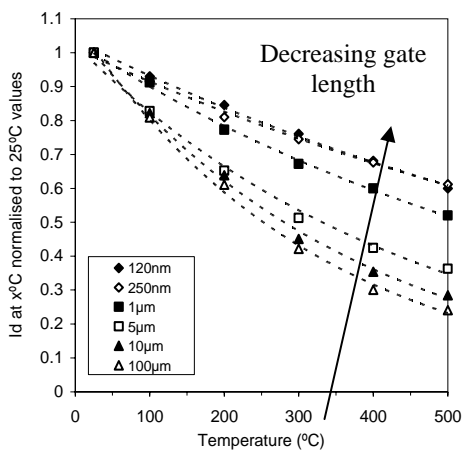
temperature dependence of the open channel drift mobility (i.e. at  $V_{gs} = 0$  V), which was extracted from measurements on the 100  $\mu$ m gate length devices [9]. The 2DEG mobility rapidly degraded from 950  $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$  to 120  $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$  between 25°C and 500°C, falling with a power law of roughly  $T^{-1.5}$ . This is consistent with the normal behaviour of polar optical phonon scattering limited mobility above room temperature.



**Figure 3.** (a) Plot of drain current at pinch-off ( $V_{gs} = -6$ V) as a function of temperature ( $T = 25^\circ\text{C}, 100^\circ\text{C}, 200^\circ\text{C}, 300^\circ\text{C}, 400^\circ\text{C}$  and  $500^\circ\text{C}$ ). (b) Temperature dependence of the 2DEG carrier mobility.

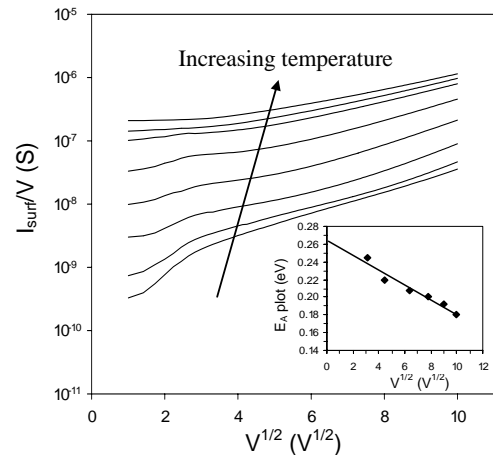
In the current literature, the 2DEG density was found to remain relatively unchanged from 25°C to 500°C and the drain current reduction at elevated temperatures (as seen in Figure 2) was attributed to the reduction in mobility [2]. However, in short channel devices in saturation, the carriers will travel at the saturation velocity and so a weaker temperature dependence than that seen for low-field electron mobility is to be expected [10]. In Figure 4, the normalized  $I_{dss0}$  saturation current is plotted against temperatures for a wide range of gate lengths, with the source-gate and gate-drain spacing both kept constant at 2  $\mu$ m. The fall in the normalized saturation current ( $I_{dmax0}$ ) with temperature was found to show a strong dependence on gate length. The

power law for the temperature dependence shown in Figure 4 (i.e.  $I_{d\max 0} \propto T^x$ ) varies with gate length, with a clear transition between the two regimes of operation for devices with gate length of around a micron. At short gate length ( $<1\ \mu\text{m}$ ), the electron velocity is saturated and a  $\sim T^{-0.5}$  power law was observed, whereas at long channel length the  $\sim T^{-1.5}$  dependence is due to polar optical phonon scattering. This implies that short channel devices will be less strongly affected by temperature than would at first sight be expected from mobility measurements.



**Figure 4.** Saturation current,  $I_{dss0}$  of different gate length devices as a function of temperature, normalized to 300K values.

These observations are entirely consistent with the Monte Carlo simulations by Bhapkar *et. al* [11]. In practice, other factors such as self-heating and substrate thermal conductivity should also be considered to optimize the high temperature operation capabilities.

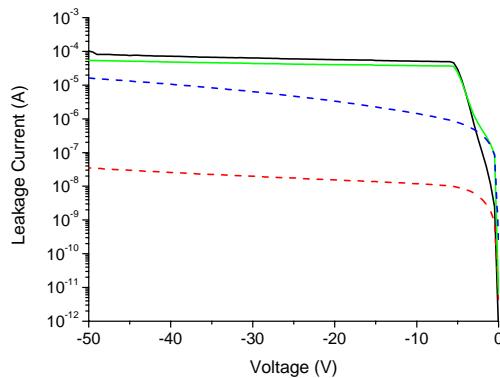


**Figure 5** Log  $I_{surf}/V$  versus  $V^{1/2}$  over a range of different temperatures for the unpassivated devices ( $T = 20^\circ\text{C}, 50^\circ\text{C}, 100^\circ\text{C}, 150^\circ\text{C}, 200^\circ\text{C}, 250^\circ\text{C}, 300^\circ\text{C}$  and  $350^\circ\text{C}$ ). Inset shows the activation energy ( $E_a$ ) plotted against  $V^{1/2}$  to obtain the trap barrier height.

The surface leakage current of the unpassivated devices can also be fitted to a Poole Frenkel conduction mechanism [12]. An exponential dependence of  $I_{surf}$  with the square root of voltage over a range of different temperatures is plotted in Figure 5. Although the distance over which the field is dropped is unknown, the extrapolated activation energy at zero-field for the process is found to be 0.26 eV. However,  $I_{surf}$  for the  $\text{Si}_3\text{N}_4$  passivated devices could not be fitted to any simple conduction mechanism, probably reflecting the highly non-linear field and the significant modification of the surface by the effective passivant. These observations tie in with the notion that the  $\text{Si}_3\text{N}_4$  contributes to the change of the charge state of the surface and hence the surface leakage current.

Doubts about the reliability of devices can

arise due to the observed inconsistency in the effectiveness of  $\text{Si}_3\text{N}_4$  in reducing ‘current slump’ due most likely to variations in surface contamination or the detailed chemical nature of the surface. In order to remove this inconsistency we investigated the use of  $\text{CF}_4$  plasma pre-treatment prior to passivation.



**Figure 6** – Bulk and surface leakage components for a device exposed to a  $\text{CF}_4$  plasma pre-treatment of 40W for 1 minute before deposition of  $\approx 50\text{nm}$  of standard  $\text{SiN}$ . The upper solid line represents bulk leakage current before passivation and the lower solid line after passivation. The upper and lower dashed lines represent the surface leakage current before and after passivation respectively.

Optimised conditions were identified where devices exposed to a  $\text{CF}_4$  plasma pre-treatment of 40 W for 1 minute before deposition of  $\approx 50\text{nm}$  of  $\text{Si}_3\text{N}_4$  were consistently effective in reducing current collapse to negligible levels in AlGaIn/GaN HFETs. Employing our novel surface leakage structure [5] enabled optimum exposure conditions to be determined to ensure minimal damage was transferred to the AlGaIn surface. Figure 6 shows the significant reduction in surface leakage current effected by the combination of optimised pre-treatment and passivation.

## Conclusions

We have demonstrated stable DC operation of AlGaIn/GaN HFETs on Si substrates from  $25^\circ\text{C}$  to  $500^\circ\text{C}$ . The temperature dependence of the saturation current is much weaker in short-channel HFETs than in long channel devices due to the reduced temperature dependence of the electron saturation velocity applicable at short channel lengths. A  $\text{CF}_4$  plasma pre-treatment prior to passivation with standard  $\text{SiN}$  is effective in reducing current collapse to negligible levels in AlGaIn/GaN HFETs. Employing the surface leakage structure enabled optimum exposure conditions to be determined to ensure minimal damage was transferred to the AlGaIn surface.

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