High-power module integrated in LTCC package

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Abstract

Low temperature co-fired ceramic (LTCC) technology has been developed for high-power applications. In this LTCC-M concept tapes are directly laminated and fired on a heat sink, which dissipates effectively the heat and increases the mechanical strength of the LTCC module. The concept has been verified by realising a demonstrator module which contains a thermal test die. Thermal simulations were also executed and the comparison between the simulations and measurements were made. This paper presents the main results from this development work for the LTCC high-power concept.

Keywords: LTCC, AlN, thermal modelling, direct lamination and firing

Introduction

LTCC is an established technology for producing integrated multilayer substrates. The system is finding new emerging applications in e.g. military, aerospace, automotive, telecommunications, and biomedical modules. One of the major advantages of LTCC technology is the use of multilayer structures, which allows the integration of passive and active components in an efficient way. Currently, there are some low-loss LTCC tape and conductor systems available, which allow the realisation of electrical circuits with good performance up to millimetre waves.

Integration of high-power devices increases the heat levels inside the substrates and, hence, efficient methods to dissipate heat from integrated circuits are needed. The most common heat dissipation method is the use of thermal vias from an IC through a substrate. A more efficient way would be to attach the IC to a heat sink by e.g. soldering. Then a good thermal expansion match is required between the IC and heat sink. In this case, the LTCC substrate is typically also soldered to the heat sink. The improvement to this method would be to attach LTCC tapes to heat sink by using a direct lamination and firing process. This method would allow the elimination of a few processing steps and enabling almost zero shrinkage of the LTCC layers in the xy-plane due to the restricting effect of the heat sink. A principle of such a module concept is shown in Fig. 1.

Direct lamination and firing attachment method has been developed in this study. In addition, a miniaturisation of the module has also been investigated. For this purpose, thin high-permittivity LTCC tape was needed for the realisation of buried capacitors. This tape would be attached on the surface of AlN substrate. Conventional low-permittivity tapes would then be placed on top of the high-permittivity tape. High- and low-permittivity tapes had a coefficient of thermal expansion (CTE) value of 9 and 7 ppm/K, respectively, which restricted the availability of heat sink materials. Thermal and thermo-mechanical modelling has been used to find suitable heat sink materials and geometries [1,2]. The best combinations have been utilised in the realisation of demonstrator modules and the main results from the work are reported in this paper.

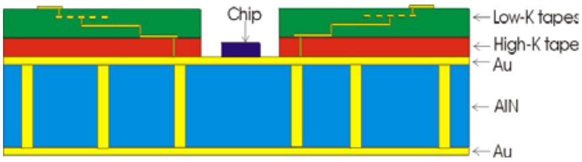

Figure 1. *LTCC concept for high-power application.*

Test materials and processing

CuW, Ni and AlN were used as base plate materials in the experiments. High-permittivity tape was CT765 (ε_r=65) from Heraeus. CT707 or CT800 were used as low-permittivity tapes (ε_r=7). The thickness of a single fired high-K tape was either about 40 or 85 µm. LTCC tapes were laminated on heat sinks with the lamination pressure of 3000 psi and temperature of 70 °C. Firing processes were made in a batch furnace. The high-K LTCC tapes required slightly higher firing temperature and a longer profile than usually needed by LTCC tapes. The samples were hold at the peak temperature of 900 °C for 3 h. The total firing process took 14-15 h.

After several experiments AlN was found to be the best option as a heat sink material [2]. Its CTE is quite well matched with LTCC tapes and it has high thermal conductivity, about 180 W/mK.

Fabrication of test module

A demonstrator module for studying the heat dissipation inside LTCC-M system was designed and manufactured. The module consisted of 2”x2” and 635 µm thick AlN substrate plated by thick-film Au paste, a single layer of CT765 tape (109 µm unfired thickness), 2 layers of CT800 (203 µm unfired thickness) and a thermal test die (from Delphi) including heating and sensing elements. In addition, the module contained also buried capacitors.

Via holes (diameter 200 µm) were punched to LTCC tapes and filled using stencil printing. The Au via fill paste used was LPA101-071 from Heraeus. After a single print the holes were not completely filled so another print was made. Au conductors were screen-printed using 325 mesh screen and Heraeus TC7102 paste. Cavities were punched to the tapes after the printing process. The tapes were then aligned on top of AlN and laminated with the aid of silicone inserts. Lamination and co-firing was made with the optimised profiles. Then the chip was assembled on AlN by using conductive adhesive (Epotek H20E). The connections from the chip to the pads on LTCC substrate were made by wire-bonding with 25 µm Au wires.

Measurement results

After firing the tapes were flat and their adhesion to AlN was good. Only few concerns were found. A cavity consisted of 2 steps. Some opens in conductors near a cavity edge were found on top of high-K tape. The main reason for this is a slight incompatibility between the conductor paste and dielectric tape. These conductor problems caused the increased resistance of the conductors and a potential reliability issue. Another problem was the posting of vias (see Fig. 2). Also this was due to a mismatch in the shrinkage between the paste and the tape. However, this did not affect the electrical performance of the vias. SEM analysis was made for the filled vias and they were filled well enough.

The resistance and capacitance values were measured. The tolerance of the capacitance values was <±4%. The dissipation factor of high-permittivity tape was 0.005 up to 17 GHz. The resistivity of the conductor was about 10^{-7} Ωm.

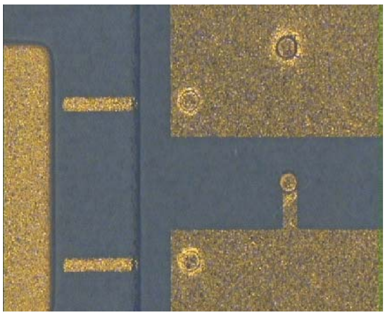

Figure 2. *Postings of vias.*

Heat distribution was also measured. The power (0.5-2.2 W, typically 2 W) was supplied to the heating elements on the chip. Temperature was measured through a diode series connection on the chip. Temperature increased quickly in a few seconds after which it increased slowly as shown in Fig. 3. The importance of the measurement arrangements was proved by temperature measurements. The modules were placed either in air or on Au-plated alumina. Obviously the cooling was much faster when the module was tightly placed on alumina plate. There were also significant differences between modules of different sizes.

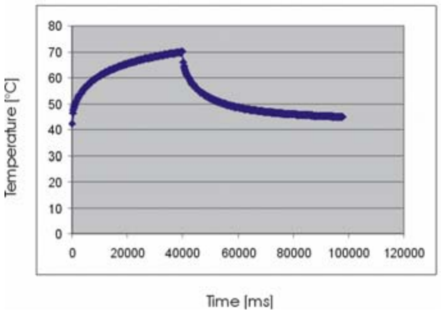

Figure 3. *Temperature profile for 12x12 mm LTCC module placed in air, 40 s heating time.*

Temperature simulations

Quite a similar geometry as shown in Fig. 1 was put into FloTherm software. The only differences were the addition of alumina plate under the AlN substrate. The low-permittivity tapes consisted of LTCC layers. The material properties used are shown in Table 1.

Table 1. *Material parameters used in the simulations.*

Item	**Size x,y,z (mm)**	**Mat.**	**Th. cond. [W/mK]**
chip	2.54x2.54x0.6	Si	117.5
glue	2.54x2.54x0.03	H20E	29
LTCC layer 1	12x12x0.085	CT765	3
LTCC layer 2,3	12x12x0.16	CT800	4.3
LTCC vias		Ag paste	260
LTCC cavity	3x3x0.405	-	-
bonding wires		Au	296
Au layer 1 (top of AlN)	12x12x0.01	Au	296
heat sink	12x12x0.635	AlN	160
Au layer 2 (top of alumina)	101.6x101.6x 0.01	Au	296
base plane (alumina)	101.6x101.6x 0.635	AlO	20

The first simulations resulted in very small temperature increases on the chip, in the range of 3-4 °C. This was due to the ideal connections between different layers. The thermal resistance of each part was calculated and the results are shown in Table 2. The formula for calculating the thermal resistance was L/kA (k=thermal conductivity, L=length and A=area). The total thermal resistance was calculated to be 0.81 K/W. If the dissipated power was assumed to be 2W, this would correspond to the temperature increase of 1.6 °C. This was quite far away from the measured results. In those measurements the temperature increase was about 28 °C. This would correspond to the thermal resistance of 14 K/W. This differs from the thermal resistance in the ideal case by 13.19 K/W. This can be thought to consist of non-idealities between different joints (such as air gaps due to non-smooth surfaces). In order to simplify the modeling, an air gap with a calculated thickness was added between the AlN and alumina substrates. By taking into account the thermal conductivity and area of air, it was possible to define the thickness of this layer. These calculations showed that suitable thickness for this layer was 48.8 µm. The main contributors to the thermal resistance were the chip and glue below it which together caused 96% of the total thermal resistance.

Table 2. *Thermal resistance of the module.*

Part	Thermal resistance [K/W]	Portion [%]
chip	0.620	76
glue	0.1603	20
Au1	0.0002346	0.028
AlN	0.0275	3.4
Au2	0.0000033	0.0004
alumina	0.003075	0.4
total	0.811078	

Parameters were varied and their effects on temperature in different locations (on chip, on AlN, etc.) were studied. The thermal conductivity of Au layer did not affect significantly when its thermal conductivity was reduced even to 2% of its maximum value. When it was dropped to 0%, then the chip temperature increased from 28 to 232 °C (the ambient temperature around the module was assumed to be 25 °C). The bonding wires and via holes did not have big effects on temperature values. Good matching was eventually achieved when the thermal conductivity of glue, Au1 and Au2 was assumed to be 90% of the initial values and the thickness of air gap was assumed to be about 40 µm. Temperatures of AlN and alumina were quite same in almost all the simulations. The analytical calculations were also made to confirm the validity of the models. Good matching was achieved with the simulation results. A typical response is shown in Fig. 4.

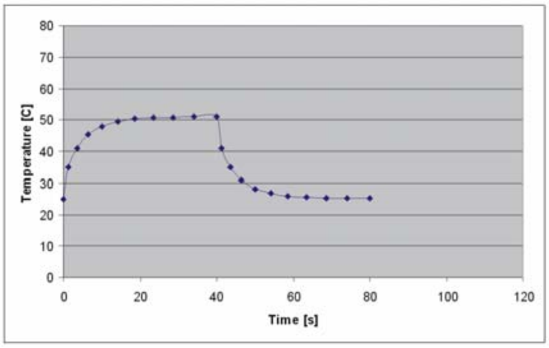

Figure 4. *Simulated temperature values for LTCC-M module (12x12 mm) when placed on Au-plated alumina.*

Summary

The LTCC-M (i.e. LTCC on metal) concept has been developed in the project. Metal in this case refers to either pure metal or insulative material deposited by metal. The studies have shown AlN deposited by thick-film Au to be the best choice in this system. In this paper modelling and manufacturing of a demonstrator module has been presented. Due to large temperature cycling during the process thermal expansion matching between the materials has to be under control. The material system currently in use results in reasonably good modules. The problems relate to the paste vs. tape compatibility which can be eliminated by developing the composition of the pastes for this system. The temperature values on the chip were measured and compared with the simulation results. A reasonably good matching was achieved when the non-idealities of the system were taken into account.

Acknowledgements

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