Fabrication of CdHgTe 16μm pitch MW infrared detectors by inductively coupled plasma etching.

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Abstract

A low damage dry etching technique has been developed using a $CH_4/H_2/Ar$ gas chemistry in an inductively coupled plasma (ICP) etcher and has been used to fabricate MW CdHgTe infrared detectors on a 16μm pixel pitch. A 16μm pitch dry etch only focal plane array with median NETD of 13mK and operability of 99.5% has been fabricated. We have also fabricated FPAs using a dry and wet etch hybrid process with a median NETD of 10mK and operability of 99.8%.

Keywords: CdHgTe, Dry Etching, ICP, RIE

Introduction

The compound semiconductor HgCdTe is the material of choice for high performance photovoltaic infrared detectors and many systems using this material are in operation today[1]. One of the major developments being pursued in CdHgTe infrared detector research is the use of small pitch arrays. The pitch is defined as the distance from the centre of one pixel to the centre of a neighbouring pixel. By reducing the pitch we are able to either increase the number of pixels in a set area and thereby increase the resolution of the detector or we can maintain the same number of pixels and reduce the overall area of a detector. For instance a full TV array with 640x512 pixels on a 24μm pitch would have minimum physical size of $188mm^2$, but by using a 16μm pitch on the same full TV array the area can be reduced by ~55% to just $84mm^2$. The reduction in physical size that can be achieved here has major consequences in the cost and weight of the final detectors. The smaller array sizes mean that more die sites are available per CdHgTe wafer, which represents a substantial cost saving in producing detectors. The use of smaller arrays allow us to use smaller lighter optical components and the reduced heat load of small arrays means that cooling engines can be of lower power. Both of these facts mean that the final detector will have a lower payload, a crucial factor in military IR system design.

Diode arrays can be made in two ways.
1) A planar method in which a pn junction is formed in an n-type homolayer by type conversion using reactive ion etching[2] or by arsenic doping using ion implantation[3]. In either case a mesa etch is not required.
2) Grown junction method where HgCdTe heterojunctions are grown onto a suitable substrate by epitaxy. In this case etched mesas are needed to define the pixels[4]. In this paper we describe the use of grown heterojunctions and mesa etching to form HgCdTe photodiodes. The current approach in fabricating photodiodes in CdHgTe is to define the mesas using wet etching. Wet etching of mesas in CdHgTe on a pitch below 20μm is not feasible as the process is

isotropic and significant lateral etching occurs leading to a reduction in the mesa top size. For instance a mesa top starting out at 14µm wide with a 2µm slot width would reduce in size to a top width of ~7µm when the slots are wet etched to the required depth. The small mesa top size would reduce the fill factor to ~19% and hence the quantum efficiency would also fall. Small mesa tops also have an impact on ease of manufacture of arrays. Any further processing to the mesa top after the mesa definition, such as opening contact windows and applying metal contacts, becomes harder to achieve, due to the limits of the lithography steps used to define the contact windows.

In order to make these small pixel pitch arrays a dry etch process is needed as it offers high anisotropy and better uniformity than the wet etched process. ICP etching is one such process that can be used for forming mesas in CdHgTe. It has the advantage over other types of dry etching, such as RIE, as it allows dry etching of material at a much lower voltage bias, and hence ions have a lower energy and cause less damage to the CdHgTe. This is achieved by de-coupling the plasma generation and ion energy by using two rf sources one for the conventional RIE and the second for creating the plasma.

We have previously reported the characterisation of our ICP dry etch process[5], and we have used ICP to fabricate working MW infrared detectors on 30µm and 24µm pixel pitches[6]. The use of ICP dry etching for mesa definition allows us to explore the use of much smaller pixel pitches than the 24µm that we have already demonstrated. We now report the extension of this work to 16µm pitch arrays fabricated from MW CdHgTe by use of ICP etching.

In this paper we describe how we have used dry etching only to fabricate mesa diodes in MOVPE grown CdHgTe heterostructures, by using a low damage etch process. We have also used a combination of dry and wet etching to define mesa diodes in CdHgTe layers. The wet etch step has two aims firstly to remove any damage that may be present at the junction surface after the dry etch and to produce a sloped profile on the mesa sidewall.

Experimental Details

MW CdHgTe heterostructures with cut-off wavelengths ~5.5µm were grown onto 3” semi insulating GaAs wafers by MOVPE. Each wafer was divided into 4 quadrants and patterned with a 16µm pitch photomask. The mask consisted of a unit cell made up of 4 pixels one of which is 14x14µm surrounded by a 2µm wide slot, these are the dimensions that would be in a full 16µm detector. Figure 1 shows a schematic plan view of the pixel layout in these devices. The active pixels in the devices are shown white in the diagram, each of these is 14x14µm separated from the neighbouring dummy pixels by 2µm slots. After the slots are etched we only apply contacts to the active pixels, which are then flip chip bonded to a 30µm pitch silicon readout integrated circuit (ROIC), this mask design allowed us to make 16µm pitch devices using an existing 30µm pitch ROIC whilst we develop a new 16µm ROIC.

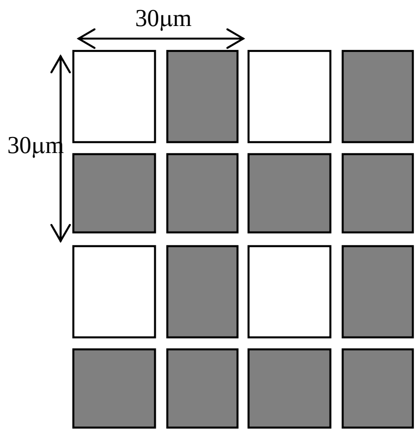

Figure 1 Schematic to show the layout of mask used for 16µm pitch dry

Two types of device were fabricated, 1) dry etch only and 2) dry and wet etch hybrids. Samples were dry etched in two machines a DSE PM2000 ICP plasma etcher or an Oxford Instruments Plasma Technology (OIPT) Plasmalab System 100 ICP dry etcher. In each case a gas mixture of CH_4, H_2 and Ar was used to etch the HgCdTe. The dry etch only devices were dry etched with a low damage process, where we minimised the impact of the physical element of the ICP etch process. The dry and wet etch hybrid devices received the same dry etch process followed by a light wet etch after the dry etch step. Wet etching of the CdHgTe was done using a weak solution of bromine in hydrobromic acid (Br:HBr). The target etch depth for both types of devices was 5.5±0.5μm. After mesa etching and removal of all photoresist the average etch depth was measured using an optical profiler. After the mesas had been defined the next processing steps were to passivate the etched sidewalls using cadmium telluride (CdTe). The dry etched only devices were passivated using MOVPE CdTe, which has the ability to coat vertical sidewalls with CdTe. The dry and wet etched devices, which have an angled sidewall were passivated using e-beam evaporation. After passivation the FPAs all had the same anneal and contact metallisation steps, and were subsequently bump bonded to CMOS ROIC and tested at 77K. Test arrays were bump bonded to leadouts and tested at 77K,145K and 192K.

Results and Discussion

Figure 2 shows an SEM image of mesa diodes formed by the dry etch only process using the DSE kit for a 16μm pitch device. The mesas have vertical sidewalls which are smooth, but a slightly rough trench base. The size of the mesa top is ~14μm^2, as defined by the photomasks since there has been no lateral etching of the CdHgTe. The large pixel size achieved means that arrays with a very high fill factor of approximately 75% would be possible for a 16μm pitch FPA with dry etch only mesas.

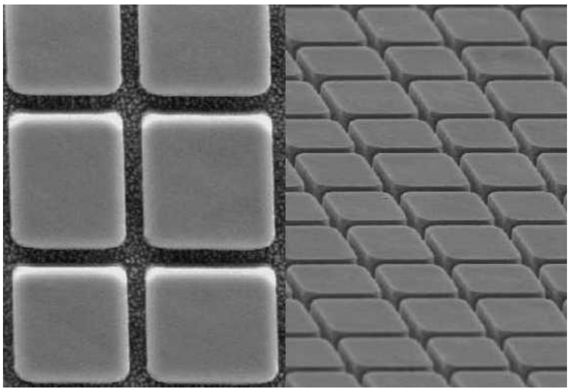

Figure 2 SEM image of dry etched mesas on a 16μm pitch array.

Figure 3 shows SEM images from a dry etch only device dry etched in the OIPT kit. The mesas have sloping sidewalls, which are smooth as is the base of the trench. The sidewalls come to a point at the base of the trench, which means that the fill factor may be higher as incident photons can internally reflect off the inside of the sidewalls into the absorber.

Figure 4 shows an NETD histogram of a 16μm pitch array etched in the DSE kit using a dry etch only process. The median NETD is 13mK and 99.5% of pixels operate at NETD < 40mK. After initial testing the array was baked at 70°C for 21 days, the NETD and number of NETD defects remained the same after this bake. We measured the IV characteristics on four different diode sizes on test arrays, which were fabricated using the OIPT dry etch kit

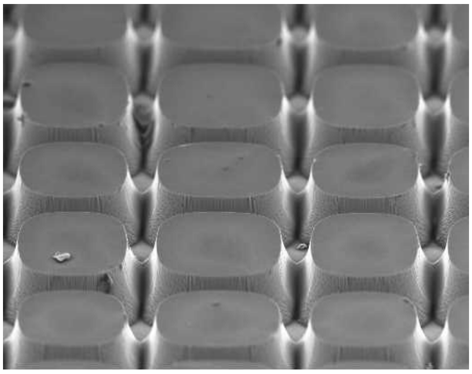

Figure 3 SEM image of HgCdTe mesas dry etched using an OIPT

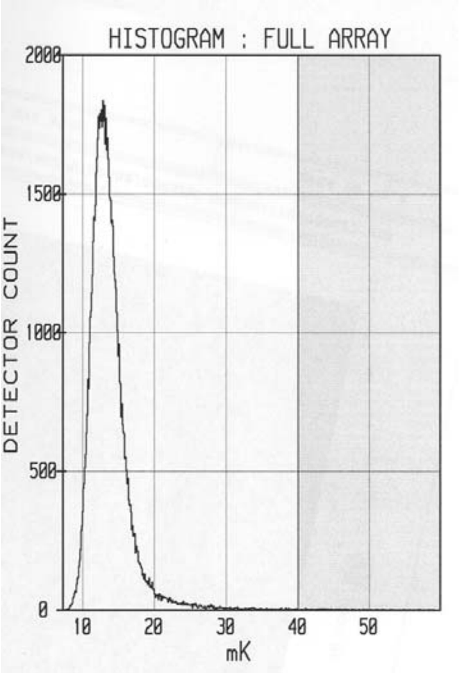

Figure 4 NETD histogram for a MW 16µm pitch CdHgTe array with dry etch only mesa diodes.

From these we calculated an R_0A product of 110Ω.cm^2 and slope of J_{sat} (saturated current density) versus P/A (perimeter over area) of 5.5 x10^{-8}A/cm at 192K for 4 with a cut-off wavelength of 4.78µm. These values for R_0A product and J_{sat} versus P/A are typical of good MW wet etched arrays at this wavelength and shows that dry etching used for these arrays has no detrimental effects on the material and device performance. The results from these arrays dry etched in two different etch kits show that it is possible to produce FPAs in CdHgTe using a dry etch only process to define the mesas. We have been able to do this by optimising the dry etch process for minimum physical damage to the CdHgTe.

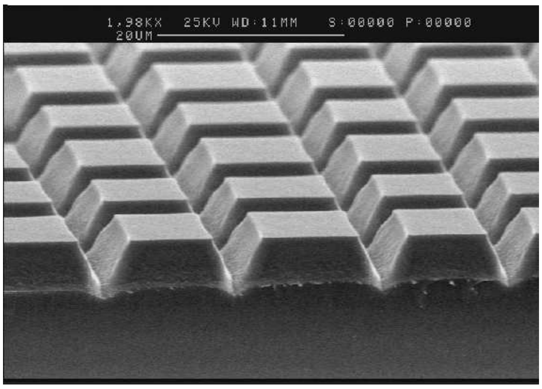

Figure 5 SEM image of mesas on a 16µm pitch array dry etched using the OIPT kit and

Figure 5 shows an SEM image of 16µm pitch mesa diodes formed using our dry and wet etch process. The mesas were dry etched in the OIPT kit, and had a sloped profile after dry etch. The SEM image shows that the mesas have a very smooth sidewall, equivalent to what is seen in wet etch only devices. From measurements taken of the mesa top size we have removed ~1.0µm from the surface of the sidewalls As a result the mesa top has shrunk to ~10µm, which is still large enough for us to apply contacts to the top of the mesa.

The NETD histogram for the array shown in figure 5 is shown in Figure 6. The median NETD is 10mK and 99.8% of pixels operate at NETD < 40mK. The FPA test results show that an array dry and then wet etched produces better diodes and fewer defects compared to an array where the diodes have been dry etched only. It is seems that the small amount of wet etching that we are doing on the dry etched devices is removing some residual damage occurring during the dry etch step.

Conclusions

We have developed a dry etch process on two dry etch kits that induces low damage to the CdHgTe layers and have used it to produce both dry etch only FPAs and dry and wet etch hybrid FPAs from MW HgCdTe on a 16µm pixel pitch. We have demonstrated an ICP dry etch only process that produces arrays with a high fill factor and FPA results that are very promising with a median NETD of 13mK and an operability of ~99.5%. We have used an ICP dry and wet etch hybrid process that has enhanced performance compared to a dry etch only array. The dry and wet etch hybrid arrays have an NETD of 10mK and an operability of 99.8%.

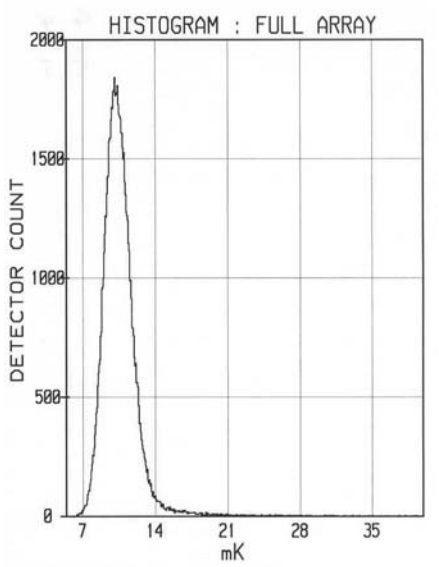

Figure 6 NETD histogram for a MW 16µm pitch CdHgTe array with dry and wet mesa diodes.

Future Work

We plan to carry out further process development of the dry etch only process on MW 16µm pitch arrays, with an aim of achieving the same electro-optic performance as our dry and wet etch hybrid devices. We are currently extending these techniques for LW CdHgTe arrays on a 30µm pitch and 24µm pitch.

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