Optical Testbed for Hybrid Optoelectronic Vector Matrix Processor for Radar Signal Processing

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Abstract

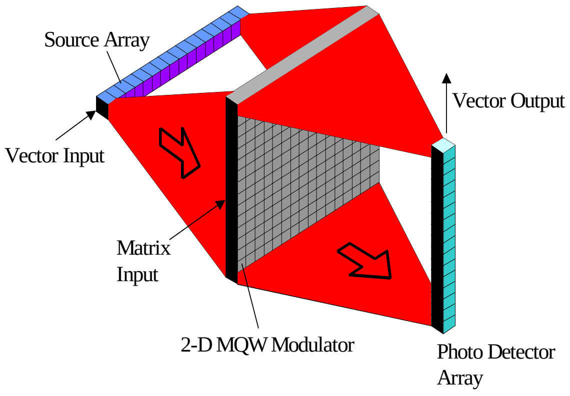
There will potentially be very large gains in computation speed and energy efficiency if a hybrid, digitally partitioned, opto-electronic vector matrix multiplier can replace state-of-art electronic processors for processing radar signals. This paper reports a novel optoelectronic architecture for a processor of this type. Realisation of a laboratory testbed system is also described. The testbed is designed to facilitate verification of concepts and techniques for processing signals having a wide dynamic range in the incoming radar signals.

Keywords: Optoelectronic vector matrix multiplier, digital partitioning

Introduction

There is a need for faster processing hardware to provide modern radar systems with advanced capabilities such as multiple hypothesis tracking, real-time clutter removal and space-time adaptive beamforming (STAP) for jammer nulling. One approach which may help to meet this need may be to use analogue processing in parts of the signal processing chain. Analogue processing can offer extremely fast computation compared to digital electronic circuitry, but has the disadvantage that it traditionally suffers from limited or slow programmability, whereas electronic devices have relatively few programming limitations. In order to optimise both processing speed and programmability, it is attractive to consider the development of hybrid processors taking advantage of the best features of both approaches.

The analogue part of the signal processing chain might be implemented using optoelectronics. Recent developments in fast (Gbit/s) laser arrays and multiple quantum-well spatial light modulators (MQW-SLM) have spurred interest in one of the simpler, yet more flexible and powerful optical processor architectures, namely the vector-matrix multiplier (VMM) [1]. A schematic view of such a device is shown below.

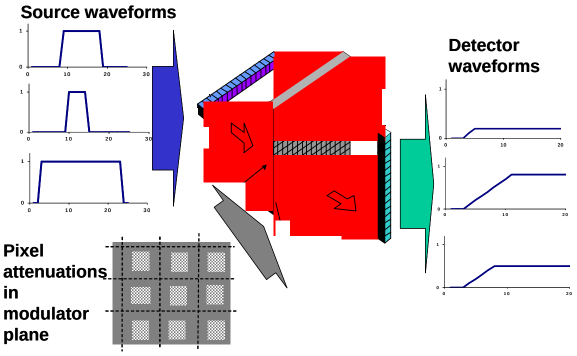


Schematic optical vector matrix multiplier

This processor works in the following manner. A set of M numbers forming an input vector are represented as optical intensities by an array of sources. The light from each source is spread over a column of M optical modulators, whose transmission represents the elements of an MxM matrix multiplying the input vector. The individual products from each row of the matrix are collected and summed on a photodetector array to form an output vector with M elements. This particular configuration is optimised for very fast throughput at moderate accuracy. The major limitation of optics in the past has been that there is a restricted dynamic range. A recently reported processor [2] operates with 8-bit digital precision. Now, it is widely quoted that dynamic ranges of 90 dB should be targeted by front-end processors for radar receivers. Since it is signal voltages, and not powers, which must be represented at the front end of the processing chain, this requirement translates into a need to perform calculations with 15-bit precision. This need can in principle be met by trading some of the vector matrix processor's vast speed for increased resolution through the use of suitable algorithms [3-5]. One particular algorithm, known as a 'digital partitioning' approach, was the subject of an earlier part of the present work [4]. This paper describes an optical testbed for performing trials of digitally partitioned, vector-matrix multiplication.

Optoelectronic system architecture

A recent report of an experimental hybrid optoelectronic vector matrix multiplier [2] employed analogue modulation of the optical sources and modulators to 8-bit accuracy, in addition to analogue optical detection. This demands excellent array uniformity, stability and linearity from the active components, to levels which are normally not achievable. The inevitable imperfections of the devices were compensated for by special algorithms. However, the present work proposes to place lower demands on such error correction methods by using more predictable digital modulation techniques at the optical sources and modulation matrix. This approach is also expected to enhance the achievable operation speed of the processor. The optical modulation methods are shown schematically in the figure below. Source modulation employs binary light levels only. Analogue signal energy is generated by time-sliced modulation within each frame period. At the matrix modulator, individual pixels are also driven for binary reflection levels, with analogue attenuation being generated by modelling matrix coefficients with pixel groups rather than single pixels. Analogue detection is achieved by photocurrent integration within a frame period.



Schematic view of optical signal flow

Main optoelectronic components

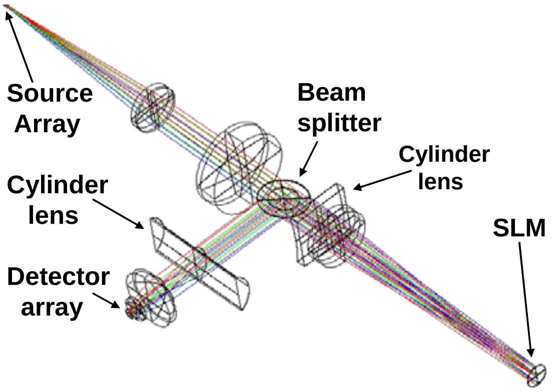
The scheme described above clearly requires the array of optical sources to cycle much faster than the frame rate of the processor. Fortunately, this need is very compatible with the capabilities of VCSEL arrays used for high speed optical communication. A linear array of 16 VCSELs emitting at 835nm was chosen for the testbed. A module containing a similar array designed for 2.7Gbit/s digital modulation was evaluated for analogue power stability and crosstalk performance during our experiments. Tests of optical, thermal and electrical crosstalk at frequencies of 125MHz and above confirmed crosstalk levels to be less than 1% of full output amplitude for the module tested. This is expected to be more than adequate for use in digitally partitioned VMM systems.

The matrix plane of practical VMM systems is most likely to rely on a reflective spatial light modulator, as this approach facilitates location of the pixel driver circuitry directly beneath each pixel. The use of digital modulation should simplify this circuitry and also should facilitate fast updating of matrix values. This latter need is expected to represent the limiting factor on the speed of fully flexible computation. Though MQW-SLMs represent the most likely solution for eventual products, these devices are currently expensive and not readily available. Fortunately, all of the basic principles of the VMM can be demonstrated at low frame rates using much cheaper, easily available liquid-crystal SLM devices. One of these devices was chosen for use in the testbed. This device was originally intended for use in an electronic display, and so it has many more pixels (1024 x 768) than are directly needed but is only capable of operating at a frame rate of 60 Hz.

In a high-speed processor, the detector ideally should be a linear array with minimum active area per element so as to maximise the frequency response. However, in order to provide the greatest flexibility, and also for system diagnostics, and finally since there is no need for high speed in the laboratory work, a board-level CMOS video camera was chosen for use in the testbed.

Optical system design

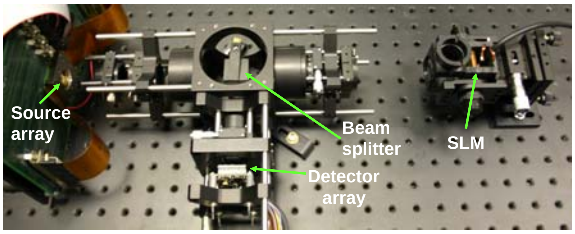
The optical system was designed using commercial ray tracing software (Zemax). Standard catalogue bulk optical elements were used throughout. Lenses were chosen to minimise the overall size of the optics and to limit relative apertures for minimum aberration. A schematic view of the system is shown in the next figure. The numerical aperture of the source array was restricted by a beam stop placed in front of the first lens. The stop is omitted from the figure for clarity. The separation between the source array and the SLM is close to 370 mm. Most of the lenses chosen are conventional achromats, since these have low optical aberration, however the fan-in and fan-out requirements require the use of cylindrical optics at two locations, as marked in the diagram. The relative apertures of the cylinder lenses were minimised, since these lenses are the major sources of aberration in the system. A high-index (ZnSe) aspheric lens was used for final focussing before the detector array so that the image size could be minimised with the best possible optical performance. Since the SLM is polarisation sensitive, a polarisation splitting prism was used as the beam splitter. In conjunction with two waveplates which have been omitted from the figure for clarity, this geometry avoided the excess losses which would have been introduced by a simple beamsplitter.



Schematic view of optical system

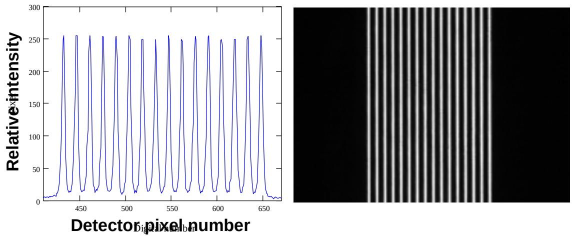
Practical Realisation

The VMM testbed was constructed on an optical breadboard, as shown in the figure below.



VMM testbed

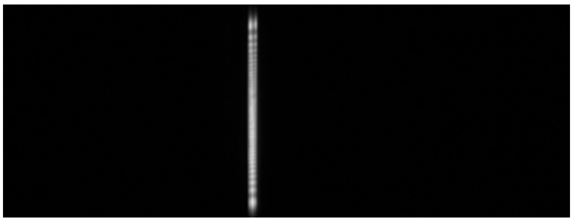
Tests of the optical performance of the testbed have shown very good agreement between the observed performance of the optics and expectations based on design work. Uniformity of the fan-out image of the VCSEL array at the SLM plane was examined by temporarily placing the camera at this position with all VCSELs switched on. The observed illumination pattern shows good uniformity and matches the design parameters well. Light from adjacent VCSELs was separated by 7 pixels on the SLM, allowing for guard bands to maintain low optical crosstalk. The figure below shows the recorded image on the right, together with a transverse intensity profile taken at an arbitrary position in the image. Low crosstalk was also confirmed by turning off one of the centre VCSELs and observing the resulting pattern.



Fan-out uniformity at SLM plane

The final image at the detector plane should ideally overlap all of the fan-out distributions from the SLM plane into a single stripe, thus automatically summing the optical powers from each row of the SLM in a small detection area. The actual image produced at the detection plane demonstrates that this has been achieved, as shown in the following figure. The width of this fan-in image is ~ 180 μm. While there is some obvious non-uniformity of transmission along the vertical axis, the pattern is the same for each column and can be compensated for in later processing.

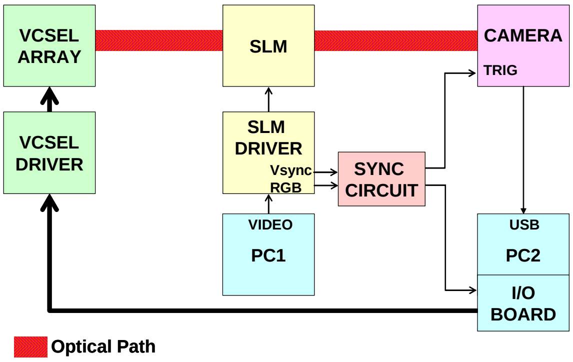
The VCSEL pulse width modulation accuracy was confirmed to be good. However, measurements using the camera suggest that some error compensation may be required for digital partitioning demonstrations, as the camera exhibits some detection nonlinearity and saturation behaviour near maximum intensity levels.



Fan-in uniformity at detector plane

VMM processor control for digital partitioning experiments

The optoelectronic system was set up for digital partitioning experiments using the control and data collection system shown in the figure below. Both the VCSEL array and the camera are operated in pulsed mode due to the operating requirements of the SLM and the camera. Each frame is initiated by PC1, which loads pixel data into the SLM driver via a video port. The SLM driver produces video synchronisation pulses which are used to trigger the camera and the timing functions of PC2 via a synchronisation circuit. PC2 controls the VCSEL array using 16 parallel output lines and gathers the final camera output via a USB port. The resulting images are processed in software, with camera pixels grouped into virtual detector elements for analysis. The finished testbed hardware arrangement is shown in the final figure, overleaf.



VMM control and data collection

Completed testbed system

Conclusions

There will potentially be very large gains in computation speed and energy efficiency if a hybrid, digitally partitioned, opto-electronic vector matrix multiplier can replace state-of-art electronic processors for processing radar signals. This paper reports a novel optoelectronic architecture for a processor of this type. Realisation of a laboratory testbed system is also described. The testbed is designed to facilitate verification of concepts and techniques for processing signals having a wide dynamic range in the incoming radar signals. Current work is employing the testbed to demonstrate key aspects of the system relevant to digital partitioning. Future work will examine approaches for miniaturisation of the optics and demonstration of high frame rates.

References

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