# GaN Power devices on Si substrates for X-band applications

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## Abstract

*GaN grown onto Si substrates offers a low cost, manufacturable route to the realisation of a power transistor technology with the potential to dramatically improve the performance of microwave power amplifiers. Here we report on developments in the epitaxial growth of GaN onto 100mm Si substrates and processing of this material for X-band devices. The role of residual strain in the ageing on GaN on Si material and device results demonstrating power densities of 2.8 Watts/mm are presented.*

Keywords: GaN, AlGaN, Si, HFET, HEMT

## Introduction

The world wide interest in GaN-based RF devices continues to grow with large programmes aimed at developing this technology in the Far East, the USA and Europe. This interest is largely based around the ability of GaN to deliver FETs with superior break down voltages and therefore higher power devices [1-5]. In comparison to GaAs FETs, a GaN based technology is capable of providing at least five times more power, at frequencies up to 40GHz, with comparable RF noise performance.

Due to the very high power capability of GaN, self-heating of devices is a significant issue and therefore the majority of GaN device development has taken place on SiC substrates which offer extremely good heat removal from devices. SiC is also a close lattice and thermal expansion coefficient match to GaN simplifying epitaxial growth. However, SiC substrates are relatively expensive (about 100 times the cost of Si substrates) and are only just becoming available in large diameters (up to 100mm) to allow current commercial device processing capabilities to be exploited.

The aim of this programme is to investigate the growth of GaN HFET structures on to Si substrates. This will offer an immediate, low cost route to commercialisation of this technology by delivering large diameter epi-wafers compatible with existing commercial device foundries. At present, the programme has focused on the demonstration of epi-structures and devices on 100mm Si substrates prior to moving to 150mm Si substrates.

In previous conference papers [6-8] we have reported on the growth by MOVPE of GaN-based HFET structures on to 100mm (111)Si substrates. Strategies have been shown, based on those used in other semiconductor systems, to overcome the large lattice (17%) and thermal expansion coefficient (54%) mismatches between GaN and Si. Utilising the techniques described growth of good quality HFET layers with

no cracking following growth has been demonstrated.

## Ageing of GaN HFET layers on 100mm (111) Si substrates

Although strain control techniques allow GaN epi-layers to be grown onto Si substrates without cracks, it is important to understand the consequences of any residual strain in the layers since this could result in ageing of the material. For wafers with significant residual strain it is sometimes observed that the sheet resistivity of the epi-layer increases during device processing and this has been correlated with cracking of the epi-layer structure as shown in Figure 1.

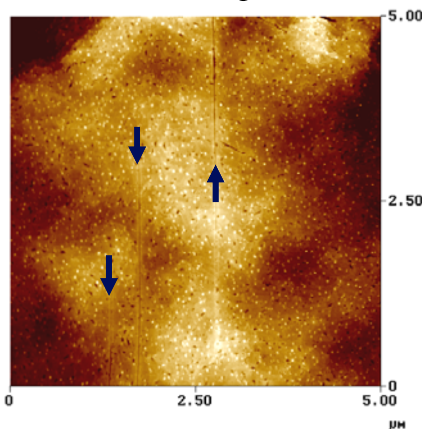


Figure 1. Atomic Force Microscope image of HFET layer surface after processing showing cracking.

Further more for layers with large values of wafer bow, ageing can also be observed during storage without processing. Figure 2 shows images of a wafer as grown and after storage for approximately 6 months. Following storage, this wafer has developed a network of line defects or cracks in its centre as shown in the inset.

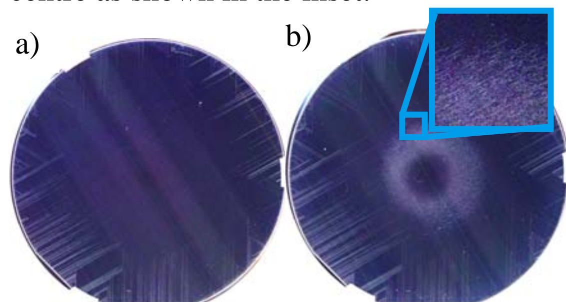


Figure 2 Full wafer images of a GaN on 100mm Si a) as grown and b) after storage for 6 months.

This ageing of the epitaxy is also associated with a change in the value of wafer bow. As grown, the bow across this 100mm wafer was around 80µm concave, reducing to about 30µm concave after storage. Ageing of the epi-layer is therefore ascribed to the residual strain in the wafers caused by the thermal mismatch of the GaN and Si during cooling from the growth temperature and resulting in wafer bow. This bowing is also a critical issue for the processibility of the wafers, as height variations across the wafer will cause problems with lithography and robotic wafer-handling in production facilities. The severity of this problem will also increase on moving to 150mm diameter substrates, as for the same radius of curvature, the value of bow increases with wafer diameter. A growth activity has therefore been undertaken to reduce and control the bowing of the wafers during growth.

## Control of wafer bow and ageing in GaN HFETs on 100mm Si substrates

Several important issues have been identified for the control of wafer bow during growth of GaN structures onto Si substrates. The first of these is temperature uniformity across the Si substrate. Any temperature variations across the substrate will result in local differences in the degree of thermal expansion of the substrate material and therefore bowing of the wafer. This may also give rise to a positive feedback situation where any bowing will cause a change in the thermal contact of the substrate with the growth susceptor, changing the heat input to the substrate locally and resulting in further wafer bowing. To provide increased control of the substrate temperature profile we have carried out modifications to the control system of our MOCVD growth reactor. This has allowed us to demonstrate a $\Delta T$ of $3^{o}C$ across the growth susceptor at the growth temperature of around $1100^{o}C$

compared to a ΔT of about 15°C before the modifications.

Along with these modifications to the temperature profile in the growth reactor, we have also modified the growth conditions for the buffer layers used to produce GaN layers on Si substrates. This has allowed the growth of HFET layers on 100mm Si substrates with less than 30µm of bow and good electrical properties (See figure 3). Examination of this material shows no evidence of cracking even at the very edges of the wafers and also no evidence of ageing after 7 months of storage. Wafers grown under these modified conditions also show no evidence of cracking during processing.

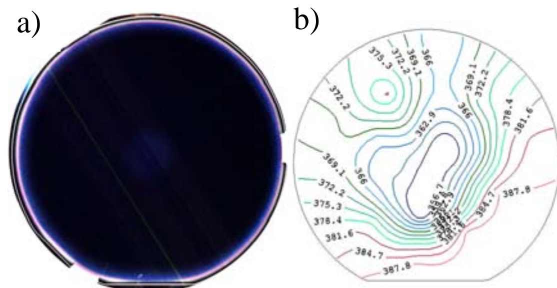


Figure 3. a) Full wafer image of an HFET on 100mm Si with less than 30µm of bow as grown and b) Lehighton resistivity map for this wafer with a mean $R_{sheet}$ of 372 ohms/sq.

## Device properties of GaN based HFETs on 100mm Si substrates

In addition to the HFET layers grown by MOCVD at QinetiQ, HFET layers on Si, purchased from a commercial source, have also been processed in to small test devices for comparison. Production of these devices uses the same process flow as that used for our standard GaN HFET devices on SiC. Photolithography is first used to define the source and drain contacts followed by e-beam lithography to produce the 0.25µm gates.

## Small signal measurements

Both types of epitaxy have given similar RF small signal device performance as shown in table 1. The cut-off frequency is comparable to that obtained for reference devices fabricated on SiC substrates, where 30-40GHz is normally obtained. In all cases the devices show good pinch-off.

| | Commercial epitaxy | QinetiQ epitaxy |
|---|---|---|
| Sheet resistance (Ohm/□) | 423±43 | 759±91 |
| Contact Rc (Ohm.mm) | 0.38±0.17 | 0.47±0.21 |
| Lg (µm) | 0.25 | 0.25 |
| Idss0 (mA/mm) | 900 | 600 |
| gm (mS/mm) | 180 | 140 |
| Vp (V) | -4.78 | -3.84 |
| $f_T$ (GHz) | 18-22 | 26-29 |
| $f_{MAX}$ (GHz) | 60 | 44-51 |

Table 1. Small signal device parameters measured for devices on MBE and MOCVD grown GaN on 100mm Si wafers.

## Large Signal RF Measurements

Large signal RF measurements have also been performed at Cardiff University on devices fabricated on both sources of epitaxy. Figure 4 shows a comparison of the dynamic load lines measured on 2x100µm devices under class A operation. In both cases, the good pinch off of the devices is seen, although the dynamic load lines are not able to access the high current "knee" region of the DC characteristics. This effect acts to reduce the total power out of the devices. The highest output power achieved on these devices was 2.8 watts/mm @ 1.8GHz which is a significant improvement on that available from GaAs devices, but still about a factor of 2 lower than that which we have demonstrated for devices processed on SiC substrates. The fundamental reason for the lower power output of the devices on Si compared to those on SiC is not known at present, but is not believed to be due to the reduced thermal conductivity of the Si substrates

since the devices tested are relatively small and therefore self heating should not be a critical issue.

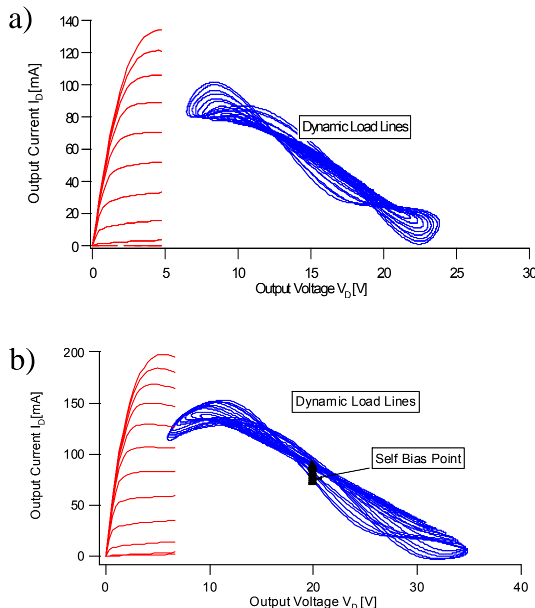


Figure 4. Fan diagrams showing the 1.8GHz RF dynamic load lines (blue) and DC-IV curves (red) for 2x100µm devices operated under Class A conditions for a) MOCVD and b) MBE GaN on Si.

## Conclusion

We have demonstrated control of the epitaxial process to reduce the bowing of GaN on 100mm Si wafers produced by MOCVD. This has successfully controlled ageing effects seen in this material during processing and long term storage. Small test devices processed in GaN on Si have demonstrated power densities of 2.8 watts/mm at 1.8 GHz which is a factor of 5 improvement over commercial GaAs-based devices (without field plates), although further development is required to match the performance of GaN on SiC devices which have produced over 5 Watts/mm. In future work we intend to migrate growth of GaN based HFETs on to 150mm Si substrates. This will provide direct compatibility of this technology with existing foundry facilities in the UK.

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