Reliability Issues for GaN HFETS

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Abstract

Some of the issues likely to affect the long term reliability of AlGaN/GaN HFETs have been studied. Pt and W refractory gates deposited by electron beam chemical vapour deposition have been compared with the more usual Ni/Au gates. Excellent DC device characteristics have been obtained with the novel gate materials, but they have not yet shown benefits over Ni/Au at high temperatures. Data on the leakage mechanisms at high temperature has been obtained which indicates that deep traps in the AlGaN layer may play a role in both bulk and surface leakage at high temperature. Finally, modelling is presented to show the effectiveness of different geometries, such as gate recess, to moderate the high electric field near the gate edge and improve on reliability.

Keywords: Gallium nitride, heterostructure field effect transistors, high temperature operation, refractory gates.

Introduction

Great strides in power performance of AlGaN/GaN HEMTs have occurred in recent years, with output power densities on SiC substrates reaching 30 W/mm at 8 GHz [1] and 12 W/mm at 10 GHz being achieved on Si substrates [2]. Passivation of the surface of the device is essential to reduce the so-called 'current collapse' [3] which causes an undesirable reduction in output current at microwave frequencies. However, passivation procedures to avoid 'current collapse' suffer from poor reproducibility which can have implications for reliability. Previous work on accelerated failure tests at high temperature [4] have shown the gate metal to be the first to fail, indicating that, initially, studies on the gate may be the best strategy to improve reliability and high temperature performance. In the previous high temperature studies, catastrophic gate breakdown was often observed [4] which may relate to high electric fields.

Here we report on the processing technologies aimed at improved reliability and reproducibility.

Experimental details

The AlGaN/GaN layers were grown by QinetiQ using metal-organic vapour phase epitaxy (MOVPE) on sapphire or 4-inch Si (111) >10 kΩcm resistivity substrates. The device structure consists of a 1µm graded AlGaN buffer layer, followed by an undoped 0.5µm thick GaN buffer and an undoped 28nm thick $Al_{0.25}Ga_{0.75}N$ barrier. The mesa device isolation (200nm depth) was achieved using inductively coupled plasma etching. Thermally evaporated Ti/Al/Ti/Au (20/100/45/55 nm) metallization was used for the ohmic contacts, annealed at 850ºC for 20 seconds under N_2 ambient. The sheet carrier density measured by capacitance-voltage was typically 9 – 13 x 10^{12} cm^{-2}, and the room temperature drift mobility found to be 950 - 1250 $cm^2V^{-1}s^{-1}$. The sheet resistance and contact resistance were determined from TLM measurements to be in the ranges 550-650 Ω/□ and 0.2-0.7 Ωmm respectively. Conventional gate contacts consisted of Ni/Au (20/200 nm) using e-beam lithography for 250 nm and 120 nm gate lengths. Ti/Au (20/300 nm) was used for bond pads.

Refractory gates of W and Pt were produced by a chemical vapour deposition (CVD) method using a Focussed Ion Beam (FIB) system with $W(CO)_6$ and $(CH_3)_3(CH_3C_5H_4)Pt$ as precursor gases, respectively. In this deposition system, energetic ions or electrons are used to break down the precursor gas which flows over the sample surface. Deposition of the metal occurs locally to the electron or ion beam, allowing 'direct write' gates down to 100 nm in length. High temperature measurements were conducted in a furnace under flowing N_2 ambient.

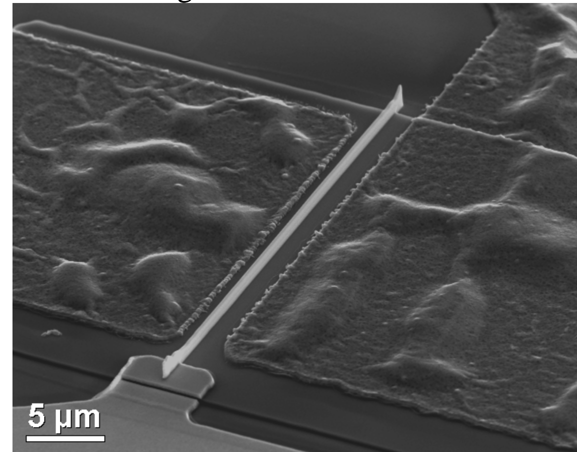

Figure 1. *Section of an AlGaN/GaN HFET with an FIB-deposited 250 nm Pt gate.*

Results and Discussion

Fig 1 shows a Pt gate AlGaN/GaN HFET deposited using the FIB technique. The gate length is 250 nm with a height of 1 µm, demonstrating the excellent aspect ratios achievable. Initial depositions using a 30 keV Ga^+ beam resulted in poor devices with little or no gate control. This was subsequently shown to be due to damage from the energetic ions, with physical evidence of sputtering and ion etching having taken place on the AlGaN surface. Additionally, "TRIM" implant simulations indicate that the Ga^+ ions will penetrate down to the channel and beyond, causing significant damage. Low energy (4 keV) electron beams gave much improved device results over the use of Ga^+ ions. However, before good *I-V* characteristics could be observed, an anneal procedure at 400°C for 5 minutes under nitrogen was required.

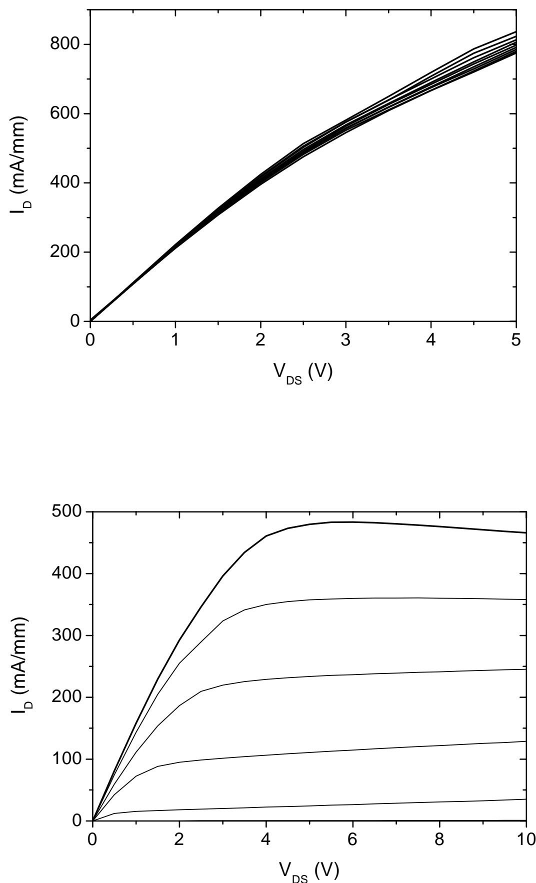

Figure 2. *I-V characteristics for an FIB-deposited 250 nm Pt gate HFET (gate width = 50 μm) (a) before anneal (b) after 400ºC anneal. The gate potential was swept from +1V to -6V, in increments of -1V.* `

Fig 2 shows the DC *I-V* characteristics of an unpassivated Pt-gated HEMT before and after the short anneal. The DC *I-V* characteristics after anneal are as good as the more usual Ni/Au gates with similar levels of gate leakage current. The anneal procedure is thought to drive off organic residue from the material surface resulting from the reaction products of the precursor material.

The W-gated devices showed similar characteristics, after anneal, but displayed lower pinch-off voltages compared to devices with Ni/Au. This is thought to be due to the higher barrier height displayed by the FIB-deposited W and may have applications in normally-off devices. The W gates in this case contain significant amounts of C due to the CVD deposition process.

High temperature electrical measurements were carried out at 500°C under flowing nitrogen in order to compare the Pt (Pt was initially chosen instead of W since it was the more developed of the two) and

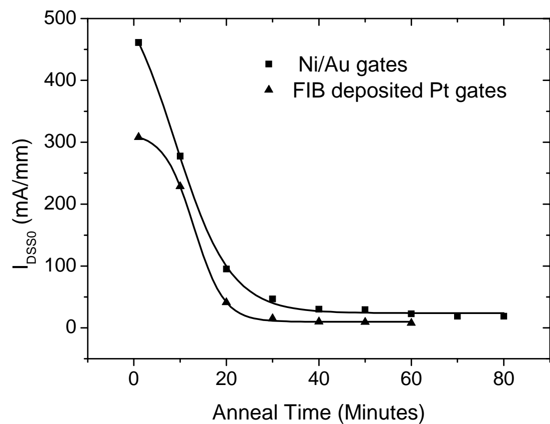

Figure 3. *Drain current at zero gate bias versus time at 500°C under flowing nitrogen.*

traditional Ni/Au gate metals. Fig 3 shows the variations of the drain current at zero gate bias, I_{DSSO}, as a function of time at 500°C. Both types of gate showed a rapid reduction in I_{DSSO} within about 20-30 minutes at which point the device effectively ceased functioning. The initial un-annealed gate-lag ratio [3] was 100% for the Pt gate compared to 65% for the Ni/Au but both deteriorated with time in line with I_{DSSO}. These changes were irreversible on cooling to room temperature, although there was a very slight recovery in drain current in the Ni/Au case. In both cases, severe damage to the gates and a lifting of the ohmic metal was observed in the SEM. No significant change in both the sheet resistance and source and drain contact resistances was observed, which indicated that gate deterioration is the most likely cause of the permanent changes. In

summary, the FIB-deposited Pt gate works as well as the traditional Ni/Au gate over a range of temperatures. However, there is no obvious improvement in high temperature performance from its use, and future work will be aimed at optimising the Pt deposition together with detailed structural and electrical analysis of the gate diode.

More detailed high temperature testing was carried out on the Ni/Au gates since these could easily be formed into the gate leakage device structure [5] which is able to separate surface and bulk leakage components. The surface and bulk (vertical) leakage currents were monitored from 300K to 500K and are shown in fig 4.

Surprisingly, the bulk leakage current decreased with increasing temperature up to 400K and then began to rise again. The explanation for this is likely to be complex, but the observed hysteresis indicates that traps within the AlGaN layer could be responsible. The surface leakage current, on the other hand, increases exponentially with temperature as expected from the activated hopping mechanism [5]. However, this current also exhibits hysteresis which indicates that the same traps are likely to control the space charge close to the gate edge and hence the injected surface leakage.

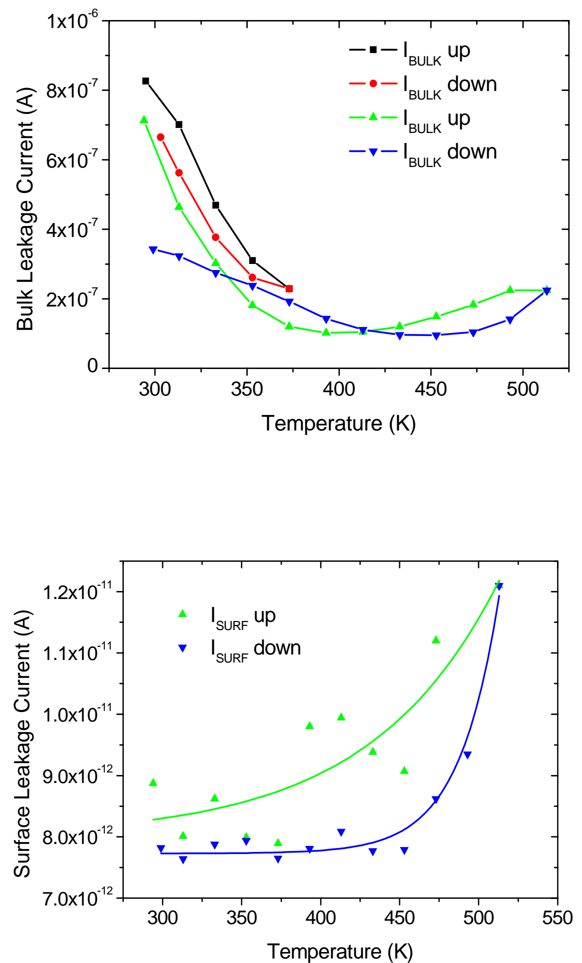

Figure 4. *Bulk and surface leakage currents as a function of temperature.*

Another factor likely to influence reliability is the pronounced large electric fields at the edge of the gate. These large fields also strongly impact on the surface leakage currents and the breakdown voltage. Electric field modelling using commercial DESSIS software is able to verify designs such as gate recess and field plate configurations with various dielectric passivation layers. Fig 5 shows calculated electric field profiles which show the positive effects of a gate recess etch through reduced electric fields at the critical gate edges. It was found that a gate edge to recess edge distance of 10-20 nm is required to minimise the field at the edge of the gate and ensure that there is a greatly reduced lateral field on the surface

outside the mesa. The resultant moderated fields will cause a reduction in injected surface currents and is expected to reduce the current collapse effect [6].

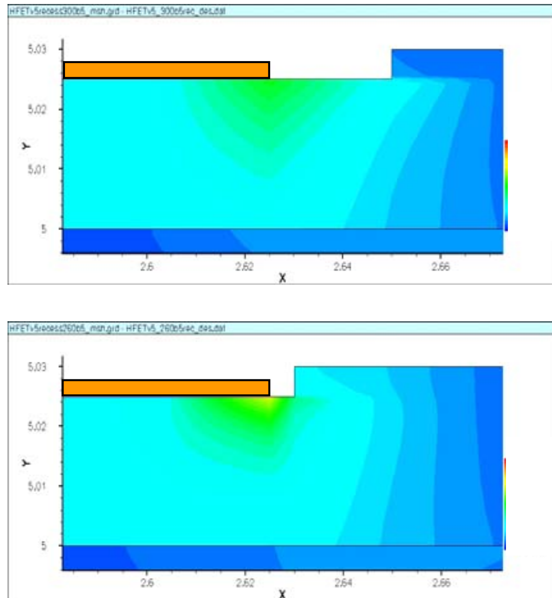

Figure 5 *Modelled electric field intensity for recess gate structures. The lighter tones represent higher field strengths*

Conclusions

We have demonstrated excellent DC operation of AlGaN/GaN HFETs with Pt and W gates using a novel CVD deposition technique. These gate metals show some promise for use at high temperatures but require further optimisation and study to assess their full benefit in this application. Deep levels in the AlGaN layer are likely to play an important role in both surface and bulk leakage currents at high temperatures.

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