3D Passive Circuit Technology for Compact MMICs

A A Rezazadeh, Lokesh Krishnamurthy, Qing Sun, Tuyen Vo, Richard Davies*

The Electromagnetic Research Centre , School of Electrical and Electronic Engineering, The
University of Manchester, Sackville Street, PO Box 88, Manchester, UK, M60 1QD,
*Filtronic Compound Semiconductors, Ltd., Heighington Lane Business Park, Newton
Aycliffe, Co. Durham, DL5 6JW

Abstract

In this EMRS DTC project at University of Manchester a number of novel multilayer passive MMIC components have successfully been designed, fabricated and tested on 2 inch GaAs substrates. By employing the new multilayer process a wide range of passive components, which are compact while maintain good performances has been successfully been demonstrated upto 40GHz. The developed passive components are currently being integrated with the pre-fabricated GaAs pHEMTs to form multilayer pHEMT 3D MMICs with significantly improved performance and functionality and lower cost. Since this technology can be integrated with any commercial available active devices (i.e., Si, GaAs, GaN, diamond...) low cost multifunctional 3D MMICs can be developed with affordable cost for future military and commercial system applications.

Keywords: Transmission lines, Couplers, inductors, Baluns, MMICs, Multilayer Circuits

1. Introduction

The recent interest in highly integrated monolithic microwave integrated circuit (MMIC) for wireless application has been driven by the expansion of the market for wireless communications and sensors. Recently, the thin-film multilayer technology demonstrates that it can be very effective in realization of miniaturization and high-level integration, which results in reduction of chip size and, thus, low cost. During this EMRS DTC project Manchester University have been carried out design, E. M modelling, fabrication and characterisation of various passive MMIC components to be integrated with commercially available active devices such as pHEMTs from Filtronic Compound Semiconductors Ltd. The outcome of this project is to demonstrate the advantages of integrating multilayer circuits with active devices to form 3D MMIC compact circuits. Figure 1 shows the concept behind this idea which is a promising technology for flexible design and cost-effective fabrication of millimetre-wave MMICs. In this structure, active devices are formed on a semi-insulating GaAs substrate, which carries multilayer of conductors and sandwich dielectrics. CPW transmission-line interconnects, passive components such as capacitors, inductors, coupler, baluns, and matching circuits are built into these multilayers. Such technology reduces the size of devices like inductors by approximately 50%, and significantly improves electrical performance while reducing cost. This technology also offers an effective separation of the application circuit process from the semiconductor active device process, resulting in a much shorter turnaround time and the flexibility of integrating various types of active devices using different semiconductor materials to form specific MMICs for the desired applications.

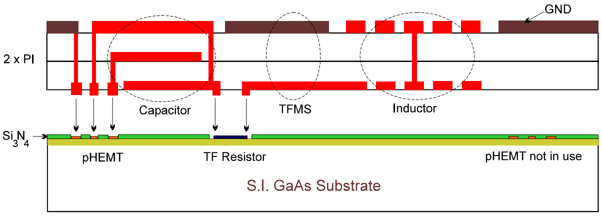


Fig. 1 Cross-sectional view of 3D MMIC pHEMTs is integrated with the passive multilayer circuits.

2. 3D CPW Transmission Lines

In realizing these multilayer structures, several processing aspects have been studied including polyimide spin, curing, etching, and metal contact formation. Full experimental details of this investigation can be found in our recent paper [1].

Three types of multilayer CPW transmission lines have been designed using the 2.5D E.M. simulator in the ADS 2004A: a conventional CPW TL with 50Ω characteristics impedance (Z_0), a high CPW TL with $Z_0 > 50\Omega$ and a low CPW TL with $Z_0 < 50\Omega$. These components were fabricated on S. I. GaAs substrates. All the transmission lines are 2-mm long. The fabricated multilayer CPW transmission lines were characterized at microwave frequencies using a Cascade Microtech on-wafer probe station and an HP 8510B vector network analyzer. The frequency dependence of transmission-line parameters such as characteristic impedance, effective dielectric constant, and dissipation loss are calculated from the measured s–parameters [2-6].

The transmission lines in conventional MMICs have a characteristic impedance of 50Ω and are widely used. However, conventional planar CPW transmission lines are lossy due to high signal loss at the edge of the conductor, which is caused by current crowding effects. Here, we demonstrate that by utilizing multilayer technology, low-loss V-shaped CPW transmission lines can be easily constructed with flexible design of impedances. For the MMICs, low-impedance transmission lines have been shown to be useful components, especially in matching networks. In conventional MMICs, the transmission lines typically have a characteristic impedance of 40–100Ω, while the microwave device themselves have a much lower input impedance. This imposes a requirement on the transmission-line design since low-impedance lines cannot readily be used. To design a coplanar transmission line with extra low impedance requires a very narrow slot between the conductors. However, at high frequency, the signal loss at the edge of the conductor can be high due to the current crowding effects.

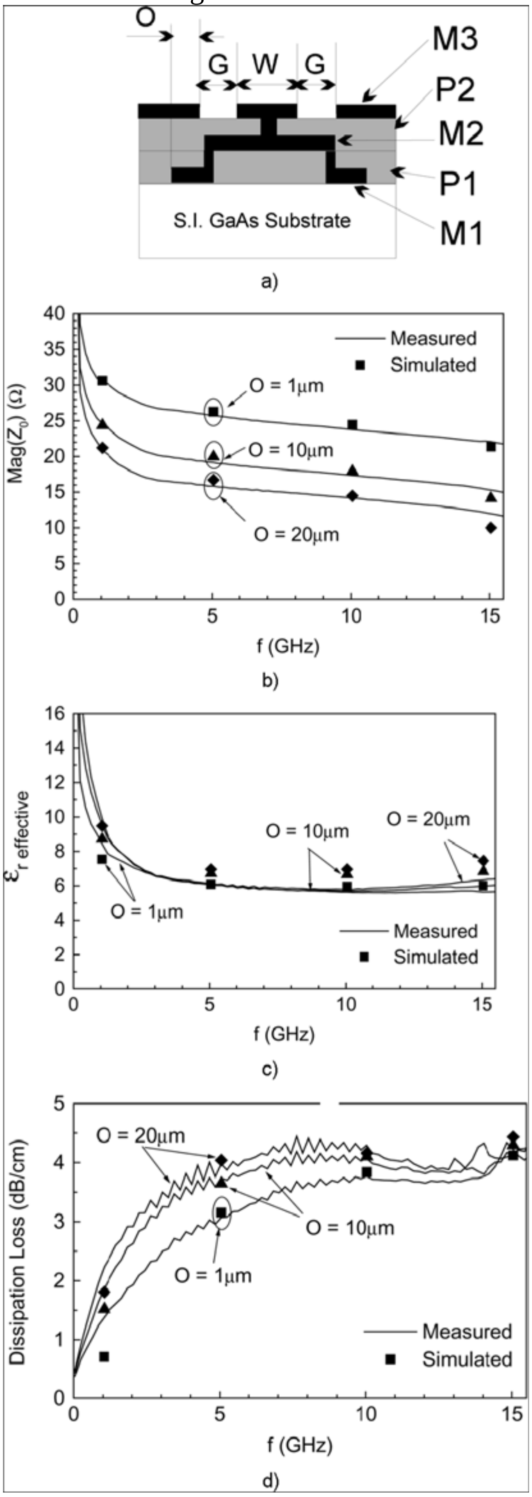


Fig. 2. (a) Cross-sectional view of a low-impedance CPW transmission line using three metal layers and simulated and measured results for its: (b) characteristic impedance, (c) effective dielectric constant, and (d) dissipation loss (W= 40μm, G =15 μm and the overlap size as 1, 10, and 20μm).

Various methods to overcome this problem and to realize low-loss lines and small compact microstrip lines have been proposed. In this study, we demonstrate that by employing multilayer structures, a low-impedance low-loss transmission line can easily be constructed. This was achieved by proper design of the transmission-line structure in which the bottom part of the centre line is overlapping the ground planes, increasing the capacitance to the ground, thus reducing the characteristic impedance. V-shaped structures also allow the current to be effectively dispersed within the conductor, thus eliminating the current crowding effect.

Fig. 2 shows the cross-sectional view of low-impedance transmission lines realized by three metal layers. The results clearly show that with appropriate overlap design of transmission lines, various low impedances can be achieved for circuit matching. For example, a 20Ω impedance was achieved with a 1μm overlap at 10 GHz. This can be even reduced to 10Ω by simply increasing the overlap to 20μm.

3. Multilayer Directional Couplers

During this project a variety of multilayer directional couplers have been designed, fabricated and tested up to 40GHz. These components were fabricated (fig 4) on 2 inch S.I GaAs substrates with thickness of about 500μm and a dielectric constant of 12.9. A typical coupler design is shown in figure 3.

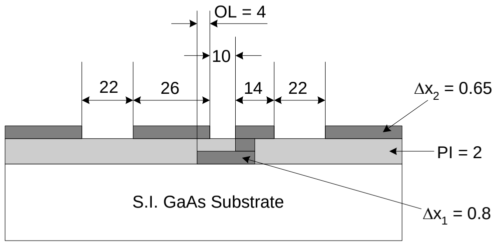


Fig. 3. Cross-sectional view of a CPW Multilayer coupler (all dimensions in μm).

The length of the multilayer directional coupler was designed to be quarter wavelength at centre frequency of 24 GHz as 1.2mm with an effective dielectric constant of 6.5. This gives a wavelength of about 4.8mm.

The dimension of the overlap area is varied and simulated using ADS Momentum software tool to observe the improvement in the performance of the multilayer directional coupler. From the simulation data at 14GHz it was found that as the overlap area increases the coupling factor improves as a result of broadside coupling. Subsequently this will also increase the isolation factor; in this design an overlap of 4μm was found to give the best tradeoff. Further improvement in the isolation factor can be achieved by using a thicker polyimide layer. For example a polyimide thickness of about 2μm provides an isolation factor of 25dB, increasing this to 3μm improves the isolation to 30dB.

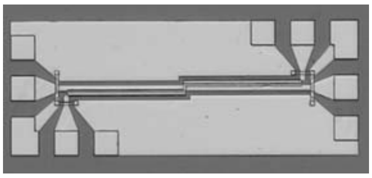


Fig 4 A micrograph of fabricated CPW multilayer directional coupler.

On-wafer s-parameter measurements were carried out using two types of calibration techniques. For straight angle ports LRRM type of calibration is used where as for the orthogonal ports SOLR type of calibration is used. A multilayer directional coupler with coupling factor of 5dB, isolation of 10dB is achieved over 10 to 35GHz frequency range with a phase angle of 90°. A good agreement was obtained for the measured and simulated results for the coupling factor (fig 5a), however there is a difference in isolation (fig 5b).

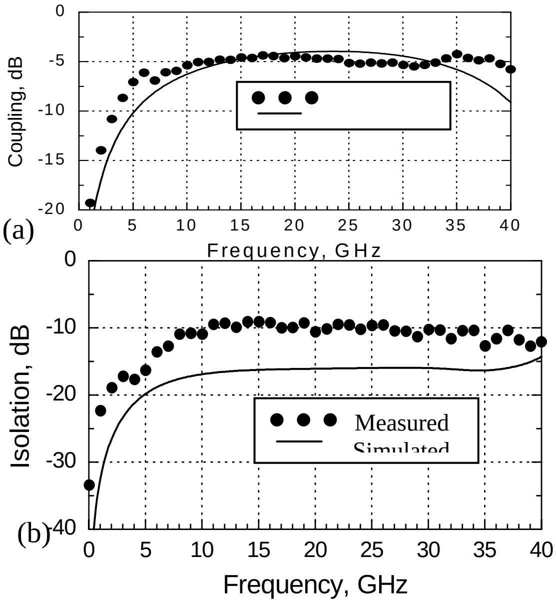


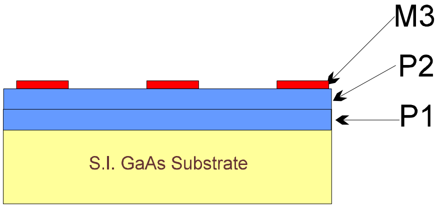
Fig. 5 Measured and simulated (a) coupling factor and (b) isolation factor for the coupler.

Although good agreement was obtained for the coupling factors (Fig 5a) the thinning of polyimide layer over the metal layers is the cause of the discrepancy in the measured and simulated results for the isolation factor.

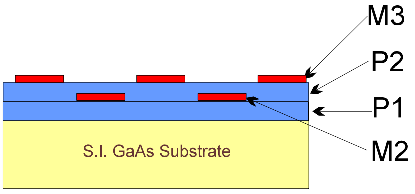
In the design optimization of passive couplers it was shown [7] that by varying the overlap area one could improve the coupling factor also by selecting appropriate thickness of polyimide the isolation factor can significantly improved. This provides a flexible design for manufacturing rather cheap microwave couplers.

4. CPW Multilayer Inductors

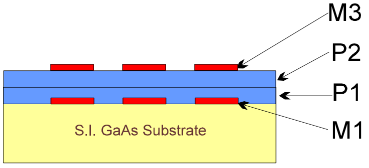
During this project we have investigated a range of CPW multilayer inductors including those of CPW based planar and microstrip based inductors.



6a) Planar



6b) Offset Stacked



6c) Overlayed Stacked

Fig 6 shows cross sections of three inductor design structures. a) 4.5 turns planar spiral (M3), b) 3+3 turns offset stacked spirals (M2-M3), and c) 3+3 directly overlayed stacked spirals (M2- M3)

These components were fabricated on S. I. GaAs substrate. Fig 6 shows cross sections of three inductor design structures. Two different types of stacked inductors were studied, one is directly overlayed and the second type is offset stacked. Offset stacked spiral inductors were realized on M2 and M3 layers. Their spacing are widened to 16μm in order to reduce the inter spiral capacitance. Similar structures with lower spiral placed on M1 are also designed, which have higher resonant frequency due to their smaller inter spiral capacitance. The directly overlayed spirals has only 9μm wide spacing and the lower spiral is placed on M3 layer instead of M2 to reduce the inter spiral capacitance.

Figures 7 and 8 show the area used by the multilayer inductors and the resonant frequency as a function of inductance and for comparison also the area and resonant frequency of conventional planar and a microstrip inductors. These results were extracted by fitting the equivalent circuit model to the embedded S-parameters. Note that the dash line represents the estimation for planar inductors. From Figure 7 it is clear that for a given inductance value a significant reduction can be achieved using multilayer inductors. The directly overlayed stacked spiral inductors take up only a quarter the space of conventional planar inductors while providing almost similar performance such as inductance, resonant frequency and Q (fig 9). The directly overlayed inductors have the highest value of quality factor, because their resistances are the smallest due to the shortest track length. Full details of this investigation can be found in [8].

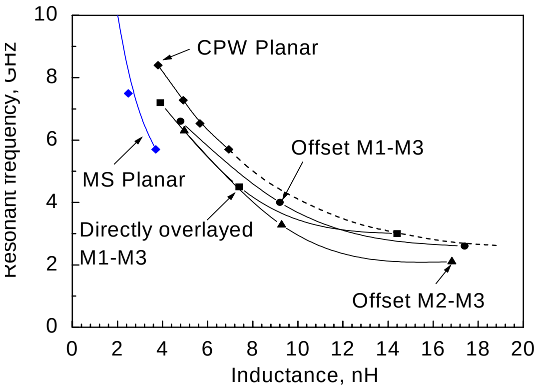


Fig.7 Variation of inductor's area with inductance for the four spiral inductors and a MS inductor.

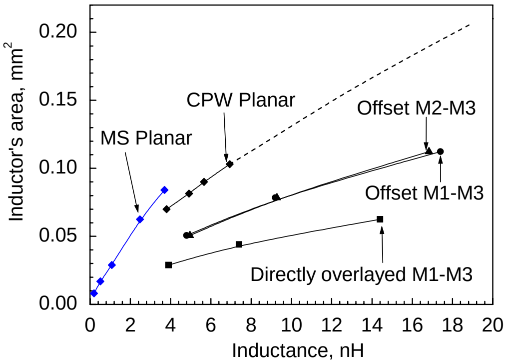


Fig. 8 Variation of resonant frequency with inductance for the four spiral inductors and the MS inductor.

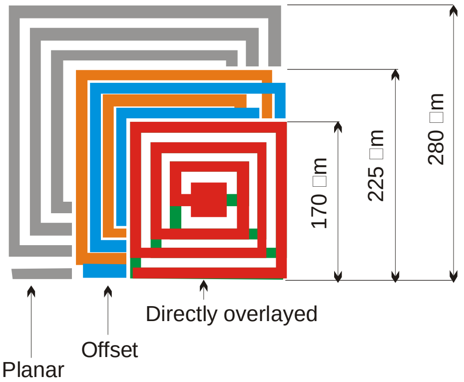
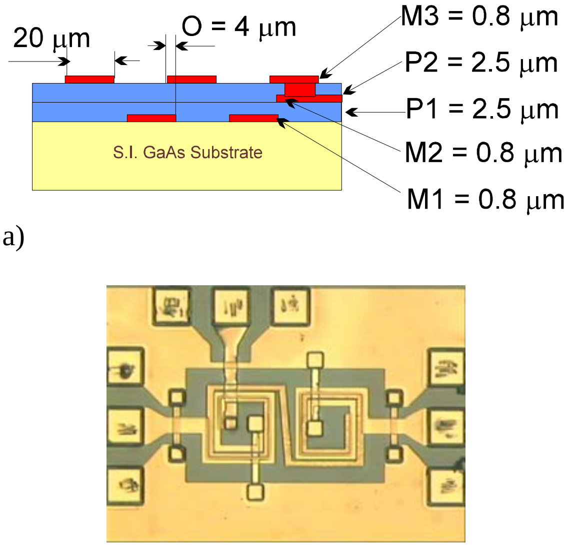


Fig 9 The area reduction in the multilayer inductors all have the same inductance.

Stacked spiral inductors can be employed in bias circuits of MMICs where the slightly higher loss and relatively low resonant frequency are little importance. They are well suited to use in applications such as lumped element matching networks for the input and output of amplifiers at lower microwave frequencies, also filter structures, which incorporate series capacitors at the centre of the spirals to produce compact L-C-L combinations.

4. CPW Multilayer Spiral Baluns

Baluns are very important components and widely used in balanced microwave circuit topologies such as push-pull amplifiers, balanced mixers, and antennas. It is used to convert an unbalanced input signal into two or more balanced output signals, or vice versa. However the ring and Wilkinson power divider based baluns are not suitable for MMIC applications due to their large [9]. In this project we have investigated a spiral Marchand baluns at 20 GHz centre frequency using CPW multilayer technology. Very compact size was realized while maintaining good amplitude and phase imbalance over a wide frequency band from 14 to 28 GHz.



a)

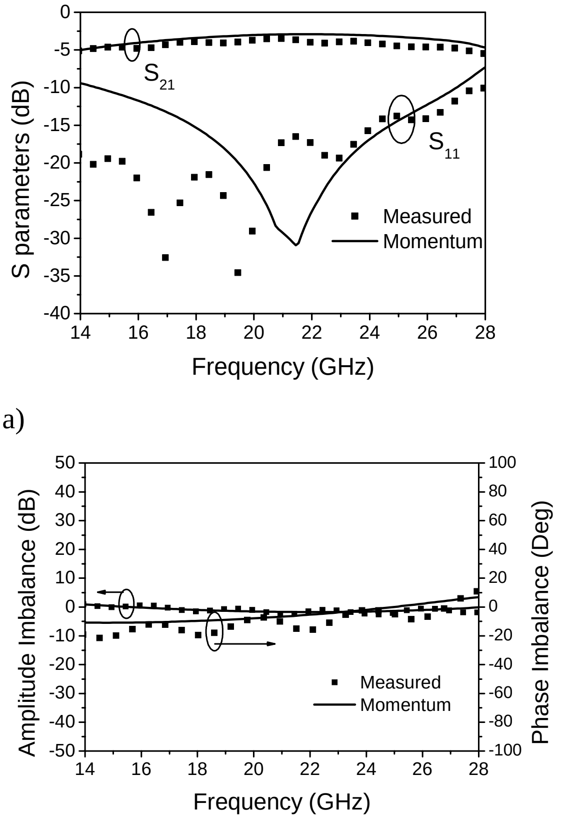
b)

Fig 10 CPW multilayer spiral balun:
a) cross-sectional view and
b) micrograph of a fabricated

Fig 10a shows the cross-sectional view of the CPW multilayer balun. The balun is formed by three-metal and two polyimide layers in sandwiched structure. The present baluns were designed based on the results of our recent study on spiral couplers [10].

Fig 11 shows the measured results of the fabricated spiral balun. The performance simulated using ADS Momentum also can be found in the same figures. From S_{11} it can be observed that the centre frequency is around 20GHz as designed. The output magnitude imbalance better than 1 dB was achieved within a frequency band from 14 to 28GHz. Also a good phase imbalance of ±10° can be seen. The insertion loss excluding 3dB power splitting loss at 20 GHz are about 1dB.

This loss is mainly due to the resistance of the long tracks and can be improved by plating them up. In overall this 3D spiral balun provides good performance over the frequency band from 14 to 28 GHz with very compact size of 0.67mm x 0.38mm. Compared to the size of planar balun it is a great improvement.



a)

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Fig 11 Simulated and measured results of the spiral balun: a) S parameters, and b) Amplitude and phase imbalance.

Fig 11a shows a good agreement between simulated and measured performance apart from a little difference of the centre frequency. This difference can be explained by different polyimide thickness of the overlap area between two spirals in practical and in Momentum simulation.

6. Integration of Passive and Active Components Issues

Some issues need to be investigated when one considers integrating the passive multilayer components with the active transistors. This is because the active transistors are normally pre-fabricated on the substrate and when considering a typical multilayer circuit to be designed only a selection of the transistors will be committed to the circuits while the remaining of the transistors will be unused. This require careful attention in order to avoid unnecessary E M coupling between various components of the circuits. In this project we have investigated the effect of unintentional horizontal and vertical couplings. For the horizontal coupling effect, a set of two adjoining transmission lines was designed and we investigated the effect of horizontal coupling on their parameters in order to identify an optimum separation where electromagnetic coupling can be neglected. Fig. 12 shows a cross-sectional view of two adjoining transmission lines on top of a 5μm thick polyimide layer stacked on the semi-insulating GaAs substrate. The transmission lines are conventional planar CPW transmission lines with the centre conductor width W = 20μm and the slot width G = 15μm and 1mm long. The separation (S) varies from 15μm (1 x G) to 90μm (6 x G).

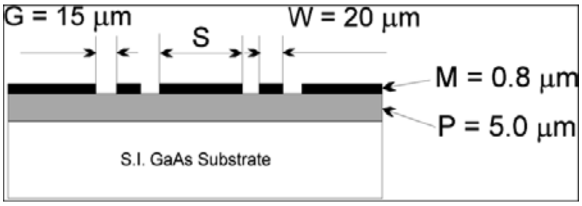


Fig. 12. Cross-sectional view of two adjoining transmission lines separated by the conductor having a width of S (W = 20 μm, G = 15μm).

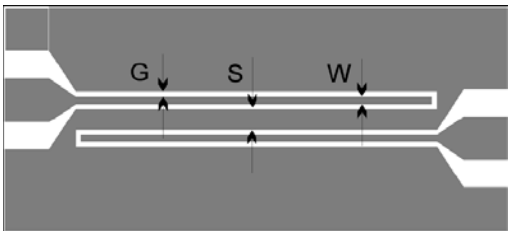


Fig. 13. Top view of two adjoining transmission lines separated by the conductor having a width of S (W = 20μm, G = 15μm).

In order to study this effect, six pairs of transmission lines with different spacing were designed, fabricated, and measured. Fig. 14 shows measured isolation between the two adjoining transmission lines as a function of separation (S). It can be clearly seen that the isolation can be improved by widening the distance between two transmission lines. However, the isolation is not improved with the spacing wider than 75 μm (5 x G), where -30dB isolation is achieved. This isolation is sufficient for most applications.

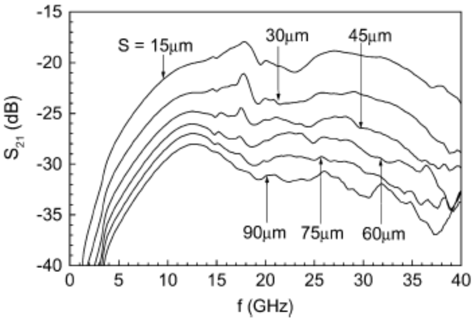


Fig. 14 Measured coupling between two adjoining transmission lines having various separation of S.

Referring to the design of the 3D CPW multilayer MMIC, it is necessary to investigate the vertical coupling between various components. This is because of the possibility of over laying of transmission lines with other conductors, which can be metal contacts of active devices such as pHEMTs. In order to keep the MMIC chip area small, the separation between transmission lines and conductor elements of different layers should be as small as possible. However, this will be a problem if there is a strong unintentional vertical coupling between them, degrading the isolation between components within the MMIC chip.

The effect of this coupling on the characteristic impedance and dissipation loss of the transmission line that crosses a pHEMT have been investigated and it is shown that how a 5µm-thick polyimide layer can provide sufficient isolation in order to minimize the effect of vertical coupling. In this study, a CPW transmission line is formed on the top metal layer and metal contacts of a pHEMT are formed by the bottom metal layer directly under a CPW transmission line. Fig. 15 shows the top view of a pHEMT employed for this investigation. Two sets of test structures were designed to investigate the effect of vertical coupling, which are shown in Fig. 13. The test structures of set (a) is comprised of a semi-insulating GaAs substrate, pHEMT devices, silicon nitrite passivation layer, and a CPW transmission line on the top level, while set (b) has two extra polyimide layers with a total thickness of 5µm above an Si N layer. The CPW transmission line has a 20µm-wide centre line, 15µm gap to ground conductors, and is 1mm long.

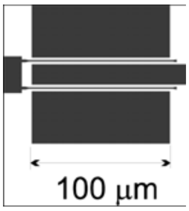


Fig. 15. Top view of metal contacts of a pHEMT used in the simulations for investigation of vertical coupling in multilayer MMICs (see Fig. 16).

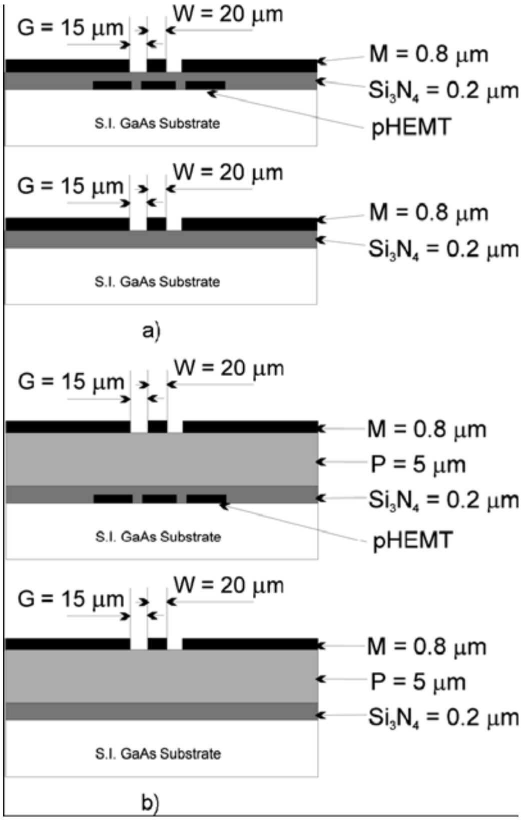
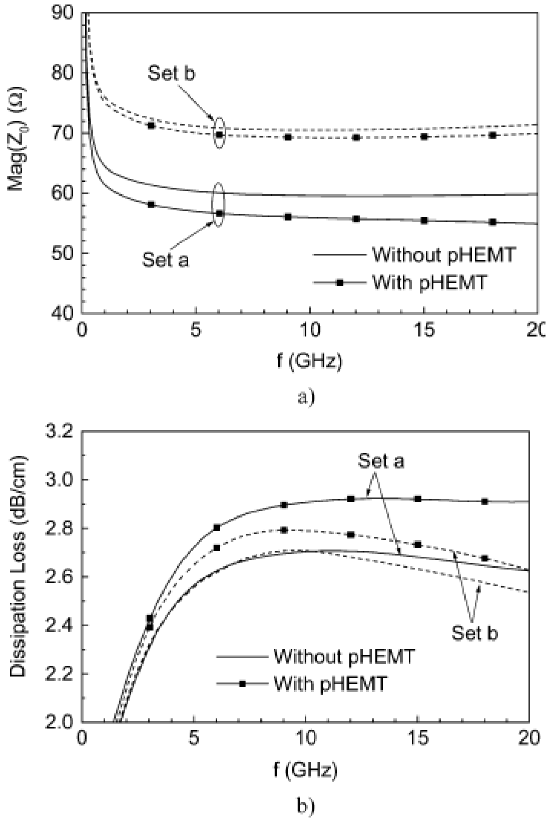


Fig. 16. Cross-sectional view of two sets of test structures for investigation of vertical coupling. Set (a) one with a pHEMT under the signal conductor and one without. Set (b), as in set (a), but with an addition of a 5-_m-thick polyimide layer.

Simulations and characterization of the two sets of transmission lines were carried out with the help of the 2.5-D electromagnetic simulator Momentum. From the results shown in Fig. 17, it can be seen that set (a) shows approximately 10% decrease in characteristic impedance and 10% rise in the dissipation loss at 10 GHz. The reduction of the characteristic impedance is due to the increase of the capacitance of the line, which is caused by additional metal contacts of the pHEMT. The extra loss is due to the fact that some of the power is coupled to the metal contacts (pHEMT) located underneath the transmission line. However, if one covers the substrate with a 5µm-thick polyimide layer, the impedance changes very slightly and the loss increases only by 3%. This effect can be understood since the thick polyimide layer prevents electric flux penetration to conductors on the GaAs substrate. This thick polyimide also provides a good isolation of the structure.



a)

b)

Fig. 17. Simulated results of: (a) characteristic impedance and (b) dissipation loss of two set of transmission lines given in Fig. 16.

These results clearly demonstrate that a 5μm-thick polyimide layer can provide sufficient isolation so that transmission lines of the top layer can cross the area above the pHEMT device without significant change of its parameters. Although careful design of the integration is necessary to ensure minimum signal loss.

7. Conclusion

This paper presents recent progress in development of compact multilayer MMIC components developed at University of Manchester. The results demonstrate that these compact structures are well suitable for low-cost, highly integrated MMICs as their occupied area are smaller than that of conventional equivalents while maintaining the same performance and thus making efficient use of MMIC chip area.

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