A Low Cost Packaging Solution for Military Applications

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Abstract

Liquid crystalline polymer (LCP) laminate materials offer a low cost solution for the packaging of GaAs MMICs and pHEMT devices in both discrete and mixed technology, Multi-Chip Module (MCM) and System in Package (SiP) configurations, for use in the harsh environments encountered in military applications. Products that could potentially benefit from this technology include modules for phased array radar applications, microwave sensors and MMIC and MCM 'drop-in' packages. Results of trials using multi-layer LCP laminates, in both modular and discrete configurations, are discussed.

Keywords: Liquid Crystalline Polymer (LCP), Packaging

Introduction

Previous published work on low cost packaging solutions for high density and high power applications, using Liquid Crystalline Polymer (LCP) laminates [1], discussed the processing of trial circuits to demonstrate the manufacture of LCP multi-layer circuits and packages. This was achieved by direct fusion bonding of the LCP laminates, or using LCP bonding films, to provide a homogenous PCB structure with both low moisture absorption and favourable microwave properties. LCP materials were initially used as a replacement for polyimides for high performance flexible circuits [2, 3].

RF analysis had been performed to assess impedance spreads associated with line width tolerance, a concern when using very thin dielectric materials and for the realisation of low loss RF transitions in multi-layer circuits. A thermal analysis had also been carried out to assess the use of high power dissipation devices mounted in several different configurations, including either direct-on-LCP with thermal grounding vias or directly to a solid metal carrier through a cavity in the multi-layer circuit. Interface options for packages had been assessed and samples manufactured to demonstrate flexible and tab interconnection techniques.

This paper presents the results from lid sealing trials on demonstration circuits and test results for both under-lid via transitions and flexible and tab interconnects, the latter taking the form of fabricated leads on discrete device packages. Further work has also been carried out investigating fusion bonding of LCP laminates to copper carriers, with the aim of eliminating epoxy interfaces from the multi-layer structure and thus, potentially, improving moisture resistance. The design of an X-Band demonstration module is also discussed which incorporates both a Power Amplifier MMIC and LNA MMIC, in the Tx and Rx paths respectively.

Technology Demonstration Circuits

Demonstration circuits, shown in Figure 1, were designed as a tri-plate structure. These incorporate under-lid transitions, on the buried layer, linked to the top layer using micro-vias in both 100um and 200um thickness versions. The circuits were manufactured at Dyconex and bonded to a silver plated aluminium carrier using silver-filled thermo-set epoxy film adhesive at Tru-lon Circuits. Cavities in the circuit, formed by laser machining, have been included to enable direct die attachment of MMICs to the metal base. Figure 2 shows a section of the multi-layer circuit.

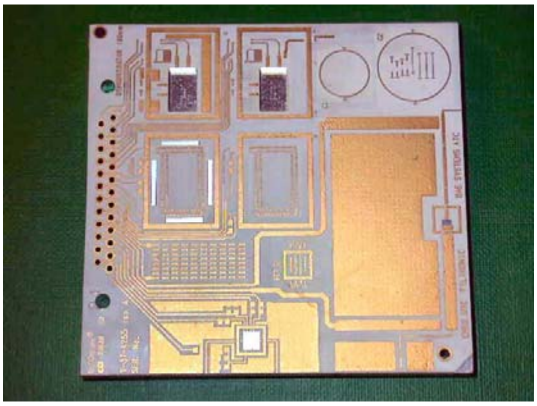

Figure 1. *Demonstration circuit mounted on silver plated aluminium carrier*

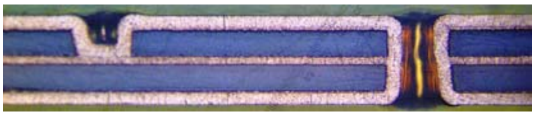

Figure 2. *Section of multi-layer LCP circuit*

Lid Sealing

Initial lid sealing process trials were performed on individual lids mounted onto a single layer RO4350 laminate PCB bonded to a copper carrier, shown in Figure 3. Two adhesives and Low Melting Point LMP) solder were trialed for comparison.

The first lid sealing adhesive evaluated was Staystik 581, a silver filled thermoplastic film with a melting range of 165ºC - 275ºC. For the lid seal process trials Staystik 581 film, 75um thick, was laser profiled to match the footprint of the lids. A process temperature, using a hotplate at 200±10ºC and a pressure of ~10psi, applied to the lid in an assembly jig utilising spring probes. The assembly was monitored using a thermocouple and held at temperature for a minimum of 60 seconds.

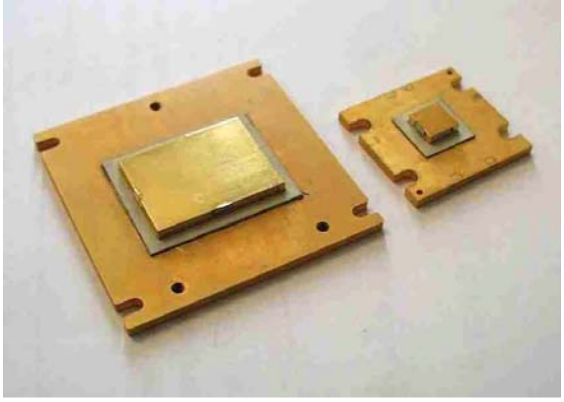

Figure 3. *Initial lid sealing process trials with individual lids on single layer RO4350 laminate bonded to copper carrier*

The second lid sealing adhesive evaluated, Epo-tek 149-6, was a silver filled thermoset epoxy which enables the material to be applied to the lid and partially cured (B-staged) and then stored for up to three months prior to assembly to package and final cure. A bead of material was dispensed onto the rim of lids and cured for 45 minutes at 75ºC in a batch oven. These were stored in a dry nitrogen atmosphere at room temperature for a period of two weeks prior to lid attachment. Subsequently they were cured for one hour at 180ºC.

Fine leak testing of individual lids yielded a leak rate of 9 x 10^{-7} atm.cm^{3}.sec^{-1} and all samples passed gross leak test (immersion in fluorocarbon fluid at 85ºC for 5 minutes) with no evidence of bubbles.

When this lid sealing process was applied to multi-cavity, multi-layer LCP circuits, however, inconsistent results were found, especially for the larger lids, shown in Figure 4. This is attributable to very subtle surface flatness inconsistencies in the lid mounting areas caused by material flow around buried tracks, typically 18um thick, during the fusion bonding process with LCP layer thickness of 50um or 100um. A means of overcoming this problem and indeed, potentially improving the overall moisture seal, is discussed later in this paper.

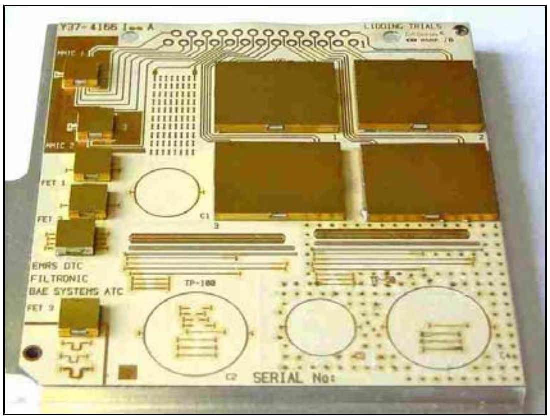

Figure 4. *Trial lid sealing on multi-cavity, multi-layer LCP circuit*

Lid Transitions

Measurements on under-lid transitions have been performed on test patterns on the multi-layer circuit using a wafer probe tester. A cross section of the test pattern, in Figure 5, shows the input and output under-lid transitions, from layer 1 to layer 2 and back up to layer 1, realised with 120um diameter micro-vias and a length of stripline.

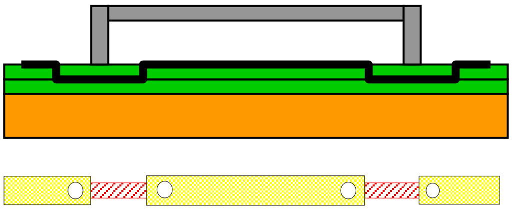

Figure 5. *Under-lid transitions*

The insertion loss, measured input to output (i.e. two transitions), and return loss plots are shown in Figure 6. Insertion loss at 10GHz is <0.5dB with a return loss of >15dB with no tuning applied.

Demonstration circuits shown in Figure 7 have been assembled with 2-20GHz broadband amplifier MMICs and a pHEMT device for further tests, which are currently ongoing.

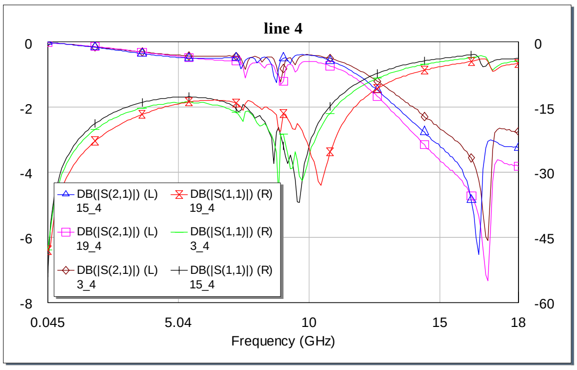

Figure 6. *Under-lid transition insertion loss and return loss measurements*

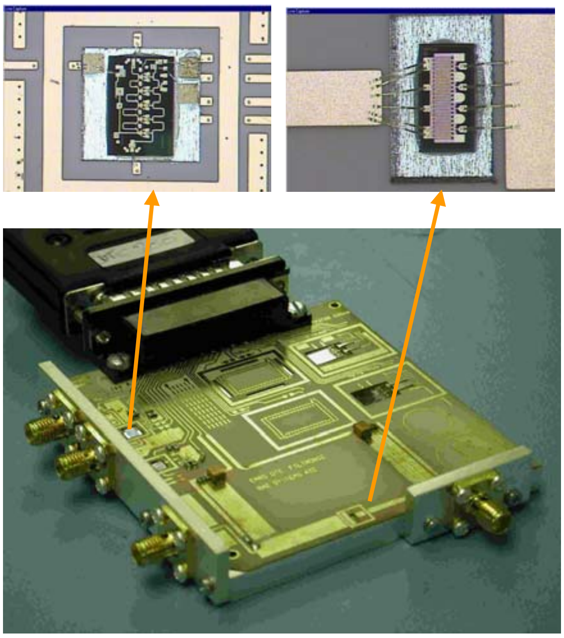

Figure 7. *Assembled demonstration circuit with broadband MMIC and FET installed*

On completion these circuits will be fitted with lids and will undergo Highly Accelerated Stress Testing (HAST) to demonstrate resistance to high-moisture environments.

Interface Options

For integrating packages or modules into motherboards, two methods of interconnect, flexible microstrip leads and integral tabs, has been evaluated. Both have the potential to be manufactured as an integral part of a circuit board or package, eliminating the need for the attachment of discrete connectors or pins.

Flexible microstrip interconnects were designed using 200um thick LCP with terminations at each end comprising a 200um diameter RF via from the top layer microstrip to a pad on the underside for solder mounting to the test board. The test fixture, with a 20mm long flexi-interconnect installed, is shown in Figure 8.

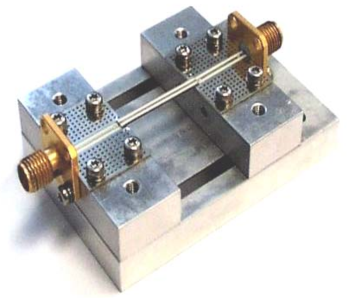

Figure 8. *Flexi interconnect circuit*

Gated return loss of the flexi-interconnect from TDR measurements gave a return loss of >18dB at 10GHz as shown in Figure 9. Improving the grounding at the interconnection by soldering a small brass carrier to the underside of the flexi lead and screwing it to the test fixture gave little improvement to performance but improved the return loss slightly at 20GHz to >15dB. This modification did, however, substantially improve the robustness of the assembly.

The 200um thick structure, although not providing the pliability for a very flexible circuit, provides sufficient flexibility for short interconnections to be able to take up any height differential between adjacent circuit boards or modules. For DC supplies and small signal applications where RF match and loss is not so critical, thinner laminate could be used, enabling high density interconnects.

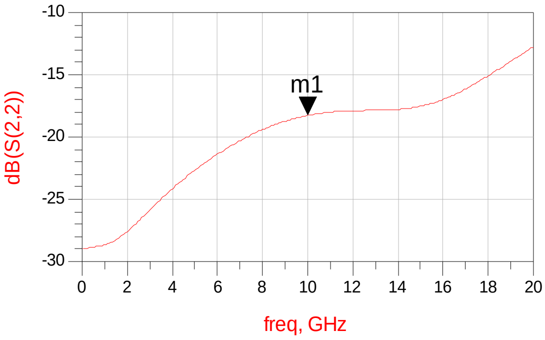

Figure 9. *Gated match of flexi interconnect*

Discrete MMIC and FET packages, manufactured by Labtech, have been used to evaluate tab interconnects. Such discrete packages could be installed in multi-chip circuits or modules, similar to the trial and demonstration circuits, to provide pre-testable / selectable devices.

The assembled FET package installed in a test fixture is shown in Figure 10. The flangeless packages were soldered into the silver plated test fixture using indium solder to ensure adequate heat sinking. These packages could, as an alternative, be manufactured with a flange to allow screw mounting to a package or baseplate.

Tests yielded a saturated power output from the via - via package of 35.6dBm, slightly less than expected. The package with galleries, however, gave 37.5dBm, which is comparable with the Filtronic ceramic packaged part (FPD4000AS). This improvement in performance is most likely attributable to lower parasitic losses as it utilises only one RF via with the gallery, at approximately the same height as the device, allowing shorter bond wires.

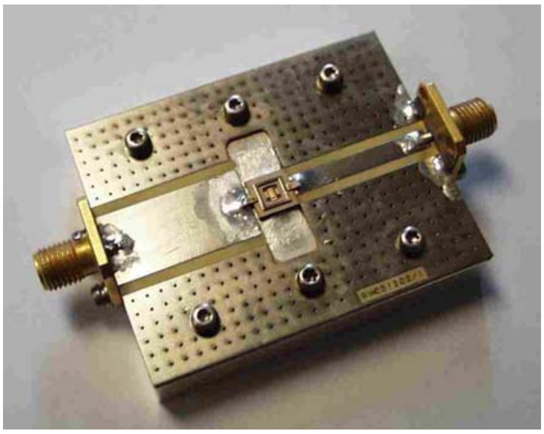

Figure 10. *FPD4000 4W pHEMT device in test fixture – partially matched*

The MMIC packages were assembled with a 2 - 20GHz broadband MMIC amplifier and installed in a test fixture shown in Figure 11. Test results gave a gain of 9dB up to 8GHz, though with a resonance occurring at 9GHz. The gain was ~1dB less than expected, with the galleried package improving the performance by only 0.25dB.

Losses in the test fixture were unknown. TDR measurements were therefore performed on a package assembled with a 50 ohm line on 250um thick alumina, placed between input and output, replacing the MMIC device and wire bonded to the package. TDR measurements on the galleried package gave a gated return loss of >20dB up to 15GHz, with >17.8dB at 20GHz as shown in Figure 12.

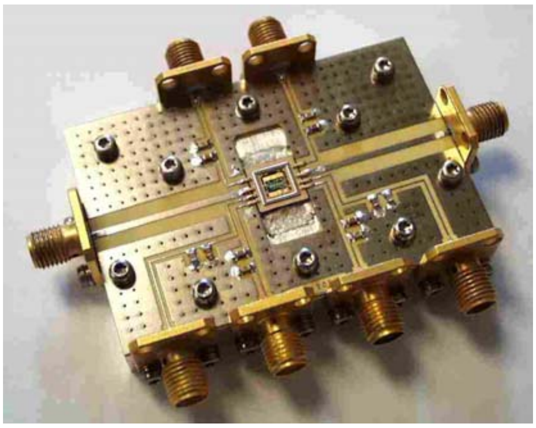

Figure 11. *Packaged FMA3007 broadband MMIC in test fixture*

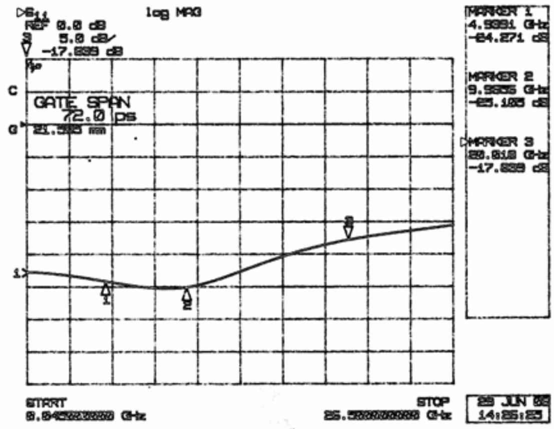

Figure 12. *TDR measurements - Gated return loss for MMIC package with 50-ohm line between RF input and output*

This was considered an acceptable performance for a package with no additional matching incorporated to tune out the parasitics associated with the interconnect transitions. For specific applications, modelling would be required to optimise the package for the frequency of operation, with any required matching integrated within the package or on-circuit.

Fusion Bonding Results

The ability to fusion bond LCP laminates directly to metal carriers would offer a homogenous LCP / carrier construction, eliminating the use of an epoxy adhesive layer. Since epoxies exhibit a relatively high moisture absorption rate of 0.5% compared to LCP at 0.04%, fusion bonding would also improve environmental sealing of circuits or packages. This is especially so for those circuits with cavities present for mounting components directly to the metal base. A challenge with the fusion bonding technique is the ability to produce ground-via holes from the top circuit layer to the RF ground or metal base. Initial trials at Tru-lon Circuits have shown excellent results as can be seen in Figure 13, where a microsection of a plated laser drilled microvia is shown (LCP fusion bonded to copper carrier).

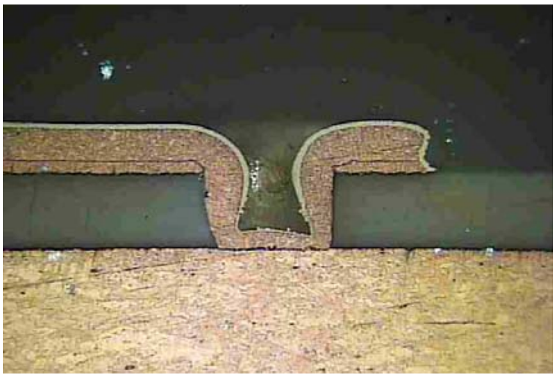

Figure 13. *Section of via hole in fusion bonded LCP laminate to copper carrier*

Further layers of LCP can then potentially be fusion bonded to this structure to make up the required multi-layer stack.

X-Band Module Design

In order to demonstrate this LCP multi-layer circuit packaging technology, an X-Band module incorporating a 10W MMIC Power Amplifier and LNA has been designed. Three options have been produced with different RF layer / transition configurations modelled using HFSS Field Solver Software. The first two, shown in Figure 14, use the transitions described for the MMIC and FET packages above and the third has a stripline transition with no via interconnects. The latter could potentially provide the lowest cost solution.

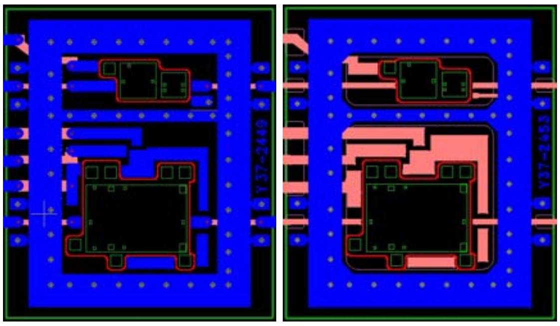

Figure 14. *Designs demonstrating Layer-1 & Layer-2 connectivity for RF Interconnect*

Conclusions and Further Work

A potential LCP packaging concept has been discussed including results of transition and package interconnect performance. Further work will include final measurements of modules, assembled with broadband MMIC's and pHEMT devices and assembly and test of the X-Band module. This will be followed by HAST testing and destructive analysis.

It is also proposed to assemble and test an X-Band module variant using LCP to carrier fusion bonding, with ground vias and an alternative lid sealing method using a soldered ring frame and welded lid to provide an epoxy free structure, offering an enhanced moisture-resistant solution.

References

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