

## Growth and Fabrication of InAs APDs

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### Abstract

*Good quality epitaxial growth of InAs and the lattice matched ternary  $AlAs_{0.16}Sb_{0.84}$  was developed using molecular beam epitaxy. An avalanche photodiode structure was designed and grown using an  $AlAs_{0.16}Sb_{0.84}$  layer to block the diffusion of minority electrons. This technique was shown to reduce the bulk reverse leakage current in fabricated devices. Further reductions in the reverse leakage current were achieved as a result of work to optimise the etchants and etching procedure followed. The chemistry of the etched surface was investigated using Auger analysis. By etching a test pixel array, the potential for fabricating small pitch focal plane arrays by wet etching was evaluated.*

Keywords: Avalanche photodiode, InAs, Leakage current, Etching

### Introduction

InAs based photodetectors can offer good quantum efficiency from the visible through to the mid infrared, with the spectral range from 1.55  $\mu\text{m}$  to 3.5  $\mu\text{m}$  of particular interest. This range has seen increasing applications including military imaging, gas sensing, free space communications, and satellite based sensing. Furthermore InAs has a band structure which differs in significant characteristics from wider bandgap III-V semiconductors. In earlier work [1] the authors have shown that this band structure can be exploited to achieve high avalanche gain at low reverse bias. As a III-V material InAs can also be grown and fabricated with relatively low costs. These characteristics make InAs an attractive material for potential manufacture of low cost, low voltage avalanche photodiodes (APDs), in a III-V material system.

APDs have rarely been reported with detection capability beyond the  $In_{0.53}Ga_{0.47}As$  cut-off wavelength of 1.7  $\mu\text{m}$ . Cadmium mercury telluride (CMT) has been used to make APDs, which have been

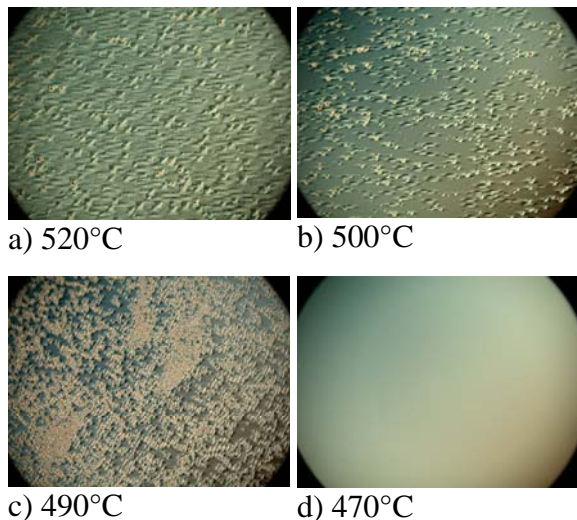
shown to have near ideal avalanche gain, and noise characteristics [2]. A CMT focal plane array (FPA) using APDs has also been demonstrated and shown to facilitate high detection sensitivity [3]. However CMT can be a difficult and expensive material to use, with controlling the compositional uniformity over the areas required for FPA applications an issue. This would make a III-V alternative cheaper and hence attractive.

APDs require higher electric fields than unity gain photo diodes which operate at near zero bias. This makes the quality of the material more critical, if the leakage current is to be minimised and device failure to be avoided. Besides optimising the quality of the bulk material other techniques for minimising the leakage current can be employed. Ashley and Elliot, employed a wider bandgap blocking layer to “exclude” electrons diffusing from the p-type cap layer of a photodiode [4], a technique which we have extended to our APD design. Since we use mesa etched devices the etch process can also have an effect on the dark current.

In this work we report on progress made towards a demonstration InAs APD FPA, with particular focus on efforts to minimise the reverse leakage current. We report findings related to growth optimisation, device design, wet chemical etching and pixel array etch tests.

### Growth and Structure Design

To determine the optimum growth conditions for InAs, a series of samples were grown at different temperatures. Following out-gassing and transfer to the growth chamber, the substrate was slowly heated up under a high As flux to determine the temperature at which the substrate began to clean up. This was observed, with the aid of RHEED monitoring to be approximately 500°C. The substrate heater temperature was then raised by 10°C for 2 minutes before the sample was taken directly to the growth temperature for the immediate commencement of the growth. The growth rate for InAs was 0.83ML/s, calibrated by RHEED oscillations on an InAs substrate. Four thick InAs samples were grown at different temperatures, optical microscope images of the resulting surface are shown in figure 1.



**Figure 1:** Optical microscope images of the surface of InAs pin wafers grown at different temperatures

The results of this study indicate that there are high levels of defects for growth temperatures at and above 490°C. For a growth temperature of 470°C the defect density is dramatically reduced, this is the growth temperature that has been used for all subsequent growth.

Minority electrons in p-type InAs are highly mobile, with long diffusion lengths. Due to this, high mobility electrons diffusing from the p-type cap can be a significant component of the reverse leakage current in pin devices. Ashley and Elliot, used a wider bandgap blocking layer at the interface to the intrinsic region to “exclude” electrons generated in the p-type cap from diffusing to the junction [4]. In our case we employ the same blocking layer technique, using lattice matched  $\text{AlAs}_{0.16}\text{Sb}_{0.84}$  (here after referred to as AlAsSb), however it is placed at the top of the p-type cap so as to block the diffusion of electrons from the contact, across the p-type cap, to the junction. The block is not placed at the intrinsic region interface because, unlike a unity gain photodiode, our APD is designed to work with optical absorption taking place in the p-type cap and electrons diffusing to the junction to initiate the avalanche multiplication. Our typical blocked pin diode structure is shown below in table 1. Reverse dark current measurements on devices with and without the blocking layer showed a reduction in the low bias bulk leakage current of more than one order of magnitude, when the block was present.

Material	Type	Width ( $\mu\text{m}$ )	Doping Conc. ( $/\text{cm}^3$ )
InAs	p	0.1	$5 \times 10^{18}$
AlAsSb	p	0.2	$1 \times 10^{18}$
InAs	p	2	$5 \times 10^{18}$
InAs	i	2	undoped
InAs	n	2	$5 \times 10^{18}$

**Table 1:** Our typical blocked pin diode structure

The growth of lattice matched AlAsSb on InAs required very careful control of the group V fluxes and substrate temperature. When a material containing a mix of group V atoms is grown there is competition between the group V species, the sticking coefficient is determined by the growth rate, substrate temperature, V/III ratio and magnitude of group V fluxes incident on the surface. Two test wafers were grown with simple single layers of AlAsSb, in order to establish the fluxes needed to obtain the lattice matched composition. The AlAsSb was grown at the optimum InAs growth temperature of 470°C. Following these trials full device structures were grown, incorporating the AlAsSb layer into pin structures. Figure 2 below shows the x-ray diffraction (XRD) spectrum of a structure grown with and AlAsSb layer. From the 180 arcsec splitting, the estimated As composition in this layer is 17%.

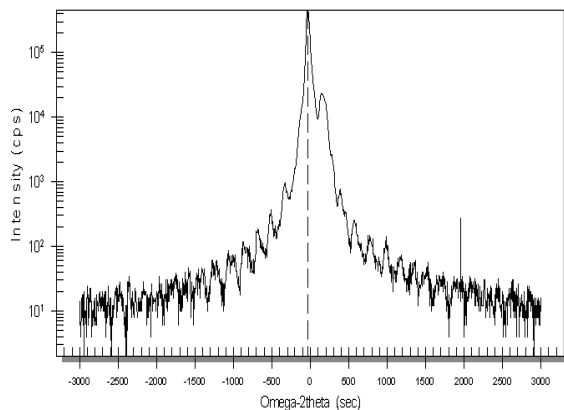


Figure 2: XRD spectrum of a full InAs pin structure with 0.2µm AlAsSb blocking layer

### Wet Etching Trial Results

The reverse leakage current in mesa etched diodes can be dominated by surface leakage current if the mesa sidewall, after etching, is electrically active. This is a particular issue for APDs which operate with high electric fields. A comparison of a range of wet chemical etchants has been made with the aim of finding an etchant which leaves an inactive sidewall, and

hence a bulk mechanism dominated reverse leakage current. Table 2 summarises the seven single and multi stage etchants trialled together with the key electrical characteristics of devices fabricated using each etch.

Etchant	Typical $J_d$ at 5V (mA/cm <sup>2</sup> )	Comment
1:1:1 HBr:C <sub>2</sub> H <sub>4</sub> O <sub>2</sub> : K <sub>2</sub> Cr <sub>2</sub> O <sub>7</sub>	2x10 <sup>4</sup>	Leakage current varies significantly from device to device.
1:8:80 H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> O	2x10 <sup>4</sup>	Good device to device consistency. Leakage current is surface dominated
1:1:1 H <sub>3</sub> PO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> O	9x10 <sup>4</sup> at 0.5V	Very high surface dominated leakage current
1:1:1 H <sub>3</sub> PO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> O followed by 1:8:80 H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> O	8x10 <sup>3</sup>	Good device to device consistency. Leakage current not surface dominated, but still not totally bulk dominated
1:1:9 HCl:H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> O	-	Would not etch InAs
2:1 C <sub>6</sub> H <sub>8</sub> O <sub>7</sub> :H <sub>2</sub> O <sub>2</sub>	8x10 <sup>4</sup>	Good consistency between devices, but leakage current high
2:1 C <sub>6</sub> H <sub>8</sub> O <sub>7</sub> :H <sub>2</sub> O <sub>2</sub> followed by 1:8:80 H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub> :H <sub>2</sub> O	2x10 <sup>5</sup>	Leakage current higher and more variable than with single stage 2:1 etch

Table 2: Summary of etch trial results ( $J_d$  is the dark reverse leakage current density)

As can be seen from table 2, with most etchants the diode leakage current was high, variable from device to device, and or surface dominated. The best results were obtained with a two stage etch of 1:1:1 (H<sub>3</sub>PO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O) followed by 1:8:80 (H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O), which created devices with the lowest leakage current density and a characteristic which was not surface dominated, but still showed evidence of a significant surface leakage current. It is interesting to note that the worst result was obtained with a single step etch of 1:1:1 (H<sub>3</sub>PO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O), however the addition of a finishing 1:8:80 etch changed this to yield the best result. The characteristic of the best sample was seen to have improved

further when it was retested five months after etching, by which time the devices had a bulk dominated leakage current with a current density  $\sim 1 \times 10^3$  mA/cm<sup>2</sup>. This observation suggests that there is the potential for surface treatment or passivation of freshly etched samples, to achieve bulk limited leakage.

To investigate the significant improvement in leakage characteristic between the single step 1:1:1 (H<sub>3</sub>PO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O) etched sample and two step 1:8:80 finished sample, Auger surface analysis was employed to try to identify the chemical composition of the etched surface. The measured Auger spectrums and the relative quantified magnitude of the Auger signal are shown in figure 3 and table 3 respectively.

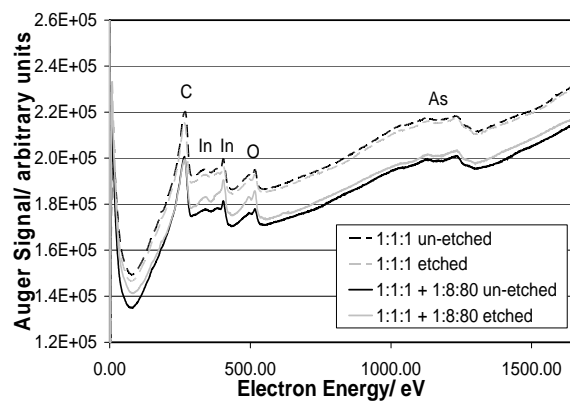


Figure 3: Auger spectrum for etched and un-etched surface areas

Surface	Relative quantified			
	C	In	O	As
1:1:1 un-etched	72	6	3.5	19
1:1:1 etched	66	<u>9</u>	<u>7</u>	19
1:1:1 + 1:8:80 un-etched	76	6	4	14
1:1:1 + 1:8:80 etched	73	6	4	<u>17</u>

Table 3: Relative quantified magnitude of Auger signal for the surface atomic species of interest

From the Auger results it can be seen that the 1:1:1 etched sample shows an increase surface concentration of indium and oxygen, with respect to the un-etched surfaces and the etched surface finished in 1:8:80. It is expected that this indicates there is a certain amount of indium oxide on the mesa surface of the 1:1:1 etched sample, which is conductive. The sample finished in 1:8:80 shows a slightly raised concentration of arsenic. The high concentration of carbon seen on the surface is not uncommon, and is believed to be organic contamination.

With the targeted final application being focal plane arrays, the ability to etch small tightly packed pixels is important. This is often best achieved using dry etching techniques, which will be investigated at a later date. However since wet chemical etching is a simple lower cost solution, it was investigated as a first option. Two etches were investigated 1:1:1 (H<sub>3</sub>PO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O) and 1:8:80 (H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O). The 1:1:1 etch was significantly anisotropic, and unsuitable for etching small pixels. The 1:8:80 etch however did prove capable of etching small pixels, to etch depths  $> 5$   $\mu$ m. An SEM view of a four pixel block with a 12 $\mu$ m pitch, etched to a depth of 5  $\mu$ m, is shown in figure 4. The mask defined 10  $\mu$ m square pixels with 2  $\mu$ m gaps.

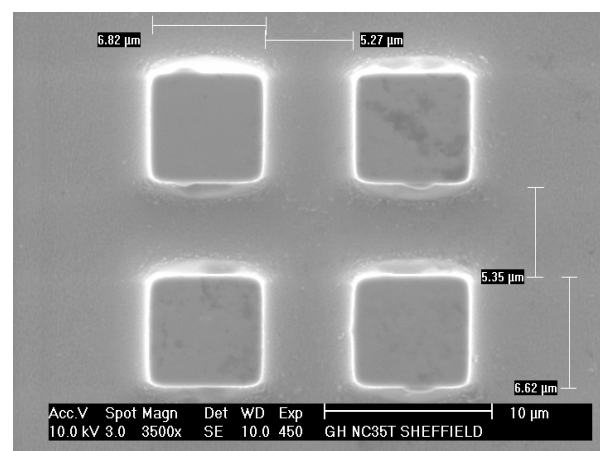


Figure 4: SEM view of a 4 pixel test array etched in 1:8:80

The 5  $\mu\text{m}$  etch depth shown in figure 4 is expected to be near the maximum mesa depth required for InAs APDs used in FPAs. It can be seen that the etch has increased the pixel gap to  $\sim 5.3 \mu\text{m}$  from the original 2  $\mu\text{m}$  defined in the mask, which has reduced the active pixel area. The fill factor of an FPA fabricated in this way would be approximately 31%. This could be easily improved by defining a smaller pixel gap in the mask, while maintaining the same pixel pitch. It is quite possible to define a 0.5  $\mu\text{m}$  pixel gap, which it is estimated would improve the fill factor to approximately 50%. Reducing the etch depth would also improve the fill factor.

### Conclusions

Wafer clean-up and MBE growth conditions for InAs and lattice matched AlAsSb have been established. It has been shown that the addition of an AlAsSb layer at the top of the p-type cap of an epitaxial pin diode can reduce the reverse leakage current, while still allowing incident photons to be absorbed in the underlying InAs p-type cap.

Trials of available wet chemical etchants have shown that the etchant used has a substantial influence on the device leakage current, with most etchants producing surface leakage limited mesa diodes. The best results do however show that it is possible to produce ideal, bulk limited devices, although further work is required to develop a process capable of doing so quickly with repeatability. Auger surface species analysis showed that the sample with the highest surface leakage current had more indium and oxygen on its etched surface than the sample with the lowest surface leakage. Finally a pixel etching trial showed that a 12  $\mu\text{m}$  pitch pixel array could be produced by wet etching. Furthermore with an optimised mask, a fill factor of approximately 50% should be expected.

This work has furthered the development of InAs APD FPAs, which maintain their promise of standard III-V manufacturing requirements, good uniformity, low voltage operation and high sensitivity.

### References

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