

UAV Collision Avoidance Radar – Build and Test

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Abstract

This paper describes an experimental radar and data recording system designed to provide the ‘sense and avoid’ capability required by UAV’s to fly in uncontrolled airspace. The radar incorporates the MIMO technique, forming multiple staring beams giving wide angular protection. Algorithms for detection in clutter, tracking, and miss-distance estimation for this radar have been developed, based on synthesised data only, hence the need for the associated data recording system. The radar and recording system comprises an Antenna Pod, Digital Transceiver and PC based radar signal processor recorder. Data captured from this radar in field experiments will assist with the verification of computer simulation results and direct further collision avoidance algorithm development.

Introduction

The utility and apparent cost effectiveness of Unmanned Aerial Vehicles (UAV) has already resulted in their deployment in a number of applications; both civilian and military [1]. It is believed that their full potential though, cannot be realised until they can operate within commercial airspace safely and autonomously.

Researchers working on “sense and avoid” or collision avoidance technology for UAV’s have approached the problem in various ways including the use of transponders [2], imaging systems [3] and radars [4-5]. Each approach has its strengths and weaknesses, but all need to pay attention to power, weight and size to be relevant to small UAV platforms.

MIMO radar [6] provides some unique advantages when applied to the UAV “sense and avoid” problem. This class of radar can produce beam information, without the associated weight of a traditional phased array or mechanically scanned aperture.

We began investigating MIMO collision avoidance radar for UAV applications using

computer simulation in previous work [7]. In this paper, we describe the construction of a prototype Radar Data Capture system that will be used to collect data. This data will enable verification of computer simulation results and assists with the further development of collision threat detection algorithms.

Antenna Pod

The Radar Data Capture system comprises three main parts: a Radar Signal Processor (RSP), a Digital Transceiver unit, and the Antenna Pod.

The Antenna Pod has been designed for ground-to-air tests only, where the requirement is to collect representative data from aircraft approaching the radar to demonstrate a warning capability. However the overall physical form of the antenna is representative of an airborne system

The structure of the radar antenna comprises four linear sub-arrays forming the four faces of a square section pod. The pod is approximately 60 cm long with an 8cm square cross-section intended for mounting in a streamlined ray-dome (Figure 1). Each sub-array face incorporates two transmitter elements and eight receiver

elements for the proposed MIMO radar technique.

The structure has been designed for the radar to switch around each face of the array in turn. This allows near spherical cover and shows the threat direction for selecting the appropriate avoidance action in a timely manner.

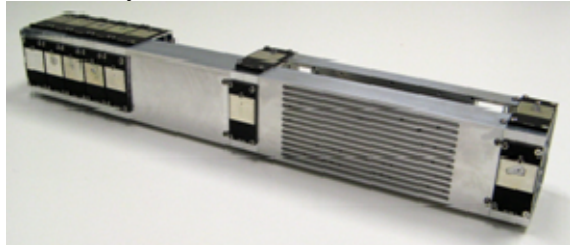


Figure 1 - Antenna Pod array.

A modular structure has been adopted with each element supporting an internal switching circuit feeding the four external antenna elements. The modules interlock to form the overall structure but can be assembled and cabled individually in sequence (Figure 2).

The transmitter modules include the power amplifier mounted piggy-back on the switching board. The receiver boards include LNA's in front of the switch network, but with no switch for LNA protection whilst transmitting, placing a constraint on transmitter power for this prototype.

Each antenna element is a printed circuit resonant cavity patch offering a very wide cover angle in the E-plane (± 90 degrees) and a suitably wide cover in the H plane (± 60 degrees). The intention was to provide the for-to-aft cover with the E-plane pattern and the circumferential cover with the four H-plane patterns. The antenna elements were designed using CST – a proprietary E-M modeling package.

Antenna elements to this design were manufactured and measured in an anechoic chamber, confirming the performance of the patch directional pattern and S parameters. A complete E-M model of the array structure has now been developed with CST showing that mutual coupling unfortunately modifies the E-plane pattern producing

nulls in the fore and aft directions. We are now proceeding with the patch antennas mounted with H plane coupling to minimise coupling for maximum transmitter power and hence target detection range.

The reduced E-plane pattern will limit the sectors from which we can collect data but this will not invalidate the aim of the proposed tests which are mainly concerned with collecting real target data to confirm the signal processing.

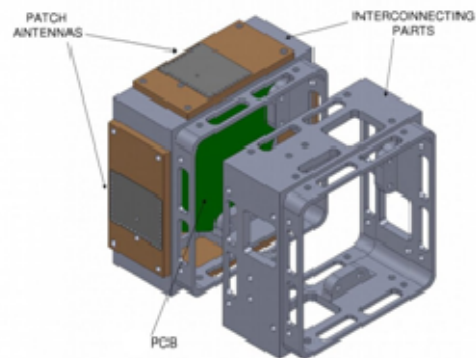


Figure 2 –Antenna Pod construction.

Digital Transceiver

Figure 3 shows a photograph of the digital transceiver hardware. This system primarily consists of signal converters (1 DAC, 8 ADCs), a signal processing capability (FPGA) and a high speed communications interface (optical Gigabit Ethernet). A Xilinx Virtex 5 SX95T FPGA performs the signal processing and manages the signal converters.



Figure 3 - Digital transceiver unit.

The FPGA also contains the command and control processor and high speed serial data interfaces.

The block diagram (Figure 4) shows the main components of the digital transceiver software. A microprocessor implemented within the FPGA handles all of the command and control operations. A real time controller is used in conjunction with a free running timer to manage time critical events associated with Coherent Processing Intervals (CPIs). The Tx pulse generator takes waveform definitions out of waveform memory, up-converts them to the digital IF (70 MHz) and sends them out to the DAC. The Rx pulse receiver block accepts sampled IF data from the ADCs and down-converts each channel to baseband. These baseband signals are then sent to the high speed link where they are packetised and transmitted to the radar signal processor. Capture memory also stores data from a nominated channel for access via the command and control interface.

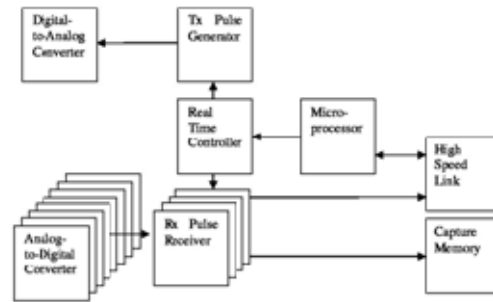


Figure 4 - Digital transceiver block diagram

Real time data communication and processing is a significant factor that impacts on size, weight, cost and power consumption. Since this radar needed to be applicable to small platforms, the RF bandwidth of the system has been kept to 6.25 MHz as a trade off between range cell size and data rate. This has allowed the radar digital communications to be implemented using COTS parts and standard protocols and has made the radar signal processing task more tractable on COTS platforms.

Radar Signal Processor

The role of the RSP is to receive information channel data from the digital transceiver and process it to determine collision threats. The RSP reported here has been built to process the transceiver information channel data offline. The three main functions of the RSP described here are pulse / Doppler / Beam processing, target detections and tracking, and collision threat processing.

The beam forming and pulse / Doppler / beam processing algorithms are based on the standard Discrete Fourier Transform (DFT) and digital filtering (Figure 5). Fundamentally, these processing stages transform the transceiver data into a format that can be used for efficient target parameter estimation. Parameter estimates made by the target detection and tracking stages are then used to determine how much of a collision threat an intruder represents.

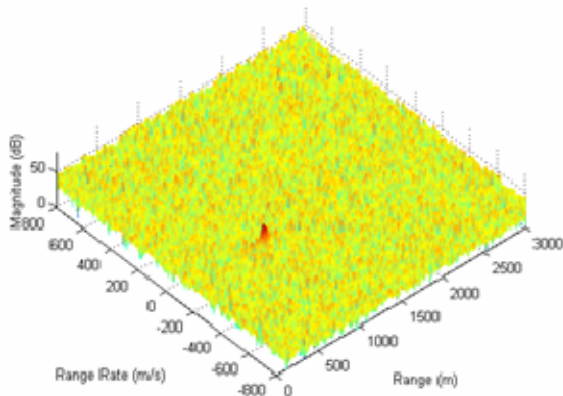


Figure 5 - Range -Doppler map for artificial beam showing 22 dB SNR detection.

Within each beam a Cell Average-Constant False Alarm Rate (CA-CFAR) algorithm detects targets in the range / Doppler scalar field by comparing each cell value to a threshold computed from the mean of local cells [8]. The CFAR threshold surface for the example beam is given in Figure 6. The algorithm determines if the signal in a cell in the range-Doppler map are above the corresponding cell in the scaled CFAR surface. If this condition is met, then a detection in that cell is registered.

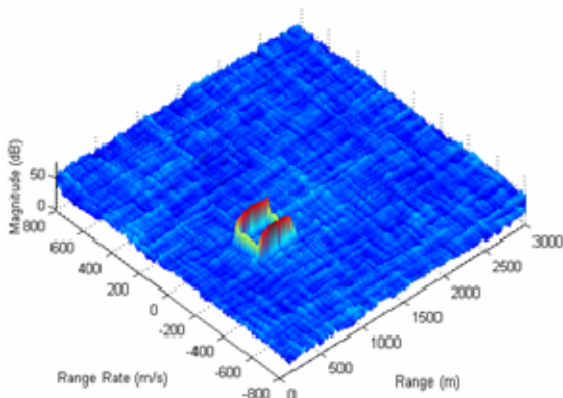


Figure 6 - CA-CFAR surface for artificial beam.

A tracker processes all of the detections declared during the detection phase. A track manager computes regions of expected detection for all tracks based on

their history. If detections are found to occupy any of these regions, the detection is allocated to the corresponding track. All remaining unallocated detections initiate new tracks. If a track has not been allocated a detection for a number of looks, the track is considered lost and the track file is deleted.

Figure 7 shows simulation results for a single intruder pass of 500m with a signal to noise ratio of 15 dB. Small 'x' symbols indicate truth data for the intruder. Tracks are shown with coloured box symbols for all looks. Note range sidelobes being tracked at high SNR.

Discussion

This paper has briefly described the construction of a prototype radar / recorder system that will be used to test and verify algorithms developed for the UAV “sense and avoid” problem. We will present field trial results recorded with the system during the conference.

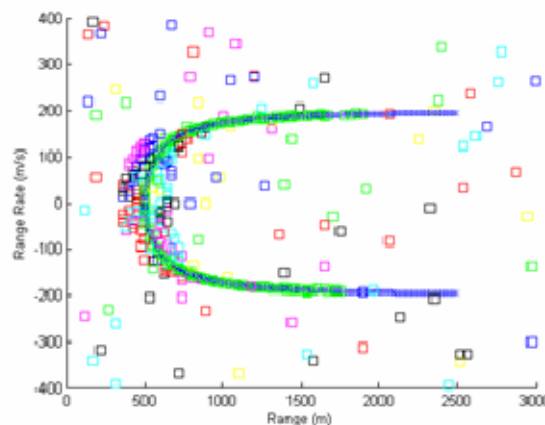


Figure 7 – Tracker simulation of intruder pass at 500m.

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