GaN X-band power transistors: A UK foundry compatible process

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Abstract

In previous years of the DTC program QinetiQ has developed the growth of GaN FET epi-layers on Si substrates in order to investigate the potential of this technology as a low cost, manufacturable alternative to GaN FET epi-layers on SiC substrates. Within the program we have demonstrated GaN FET devices on Si which have power densities of 2.8W/mm and f_T of more than 26GHz suitable for X-band applications. In this paper we report on the transfer of the growth process to 150mm Si substrates, representing the critical element required to allow GaN on Si technology to be processed in the commercial foundry facilities available in the UK.

Keywords: GaN, AlGaN, Si, HFET, HEMT

Introduction

Over the last few years GaN power devices and MMIC circuits have been produced in Europe with demonstrated performance advantages over state-of-art GaAs devices [1]. This is fundamentally due to the superior break-down voltages that can be achieved for GaN devices. As a result of this, GaN power transistors have been shown to have advantages including at least five times more power densities at frequencies up to 40GHz, whilst providing comparable RF noise performance to GaAs devices [2-5]. This excellent performance has also lead to a number of devices based on GaN technology becoming commercially available from the USA and Japan [6-8].

Despite the demonstrated performance benefits of GaN technology, its wide-spread exploitation for military and commercial applications is hampered by the cost of producing devices. This is partly due to the high cost of semi-insulating SiC substrates, but mainly due to the limited wafer diameters available which restricts ompatibility with existing commercial foundry facilities.

If comparable device performance could be achieved for GaN growth on Si substrates this could instantly reduce substrate costs by a factor of about 100, but more importantly remove the restrictions on wafer size since Si wafers are readily available up to 300mm diameter. The aim of this programme has been to investigate the feasibility of growing GaN Field Effect Transistor (FET) structures onto Si substrates and assess device performance.

Performance of GaN on Si devices

Initial work in this programme has concentrated on small wafer diameters (50mm and 100mm) in order to demonstrate the performance of GaN FETs on Si substrates. In previous conference papers [9-12] we have reported results on the growth of crack-free epitaxial layers and the processing of devices. An example of such a device is shown in Figure 1 which gives the DC and RF load pull measurements of a GaN FET device produced on a 100mm Si (111) substrate.

The device shown in figure 1 delivered a power density of 2.8W/mm with a power added efficiency of 35.7% and a f_T of 26-29GHz. A power density of 2.8W/mm represents a factor of 2 decrease in power density compared to similar devices on SiC substrates, but a factor of 3 increase in power density compared to state-of-art GaAs devices.

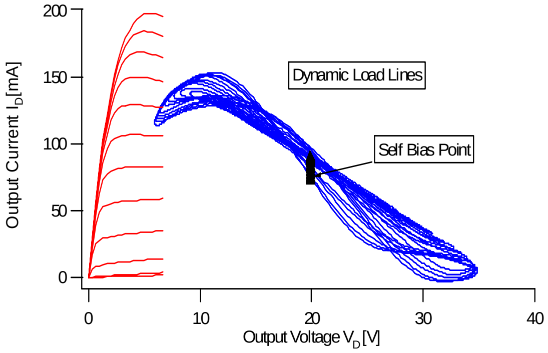

Figure 1. Fan diagram showing the 1.8GHz RF dynamic load lines (blue) and DC-IV curves (red) for a 2x100μm device operated under Class A conditions for a GaN on Si FET (measured at Cardiff University).

Further developments

Having demonstrated a significant performance advantage over GaAs devices, the next stage of development for the commercial exploitation of FETs on Si has been to deliver FET layers on larger, 150mm diameter substrates. This will provide compatibility with the commercial foundry facilities in the UK and potentially an immediate, low cost route to commercialisation of GaN power devices.

During this year of the DTC programme, QinetiQ has completed the installation of a new MOCVD growth reactor which is capable of growing FET structures onto 150mm (111) Si substrates. An important aspect of the new reactor is a suite of in-situ monitoring tools which allow a detailed understanding of the growth process and its impact on strain in the GaN layers. The in-situ tools include an optical reflectometer to measure growth rate, a pyrometer and photodiode array to measure the absolute temperature and temperature uniformity and a wafer bow monitoring system which measures the curvature of the wafer during growth. The programme of work has used these tools to transfer the growth of FET structures to 150mm substrates and to further reduce wafer bow. This is important because for a constant radius of curvature, the magnitude of wafer bow increases as the square of wafer diameter. The bow of the wafers has an impact on the processibility of the material and to provide full compatibility with commercial foundry facilities a target of ≈ 50μm of bow is required across the 150mm wafer diameter.

Initial growths of FET calibration layers onto 150mm (111) Si substrates in the new reactor showed considerable variability from run to run. Table 1 shows the wafer bow after growth for several 150mm wafers produced under nominally identical conditions. From Table 1 it can be seen that whilst values of bow as low as 5μm can be achieved, values of up to 102μm are also seen.

Layer ID	Bow parallel to flat (μm)	Bow perpendicular to flat (μm)
Wafer 1	-47 Concave	-59 Concave
Wafer 2	-3 Concave	+5 Convex
Wafer 3	-91 Concave	-102 Concave

Table 1 Wafer bow measured parallel and perpendicular to the wafer flat for GaN on Si structures with nominally identical buffer layers.

This variation in final wafer bow has been traced to a variation in bow of the starting substrates. Figure 2 shows the results of bow measurements on an initial batch of 25 substrates before growth. The variation in bow for these substrates ranges from +55μm (Convex) to -35μm (Concave).

A second batch of substrates were then obtained from a second supplier and these show a much tighter variation in starting bow, ranging from only +22µm to -6µm as shown in figure 3. This illustrates the need for tight control over the specification of the starting material in order to provide good process reproducibility.

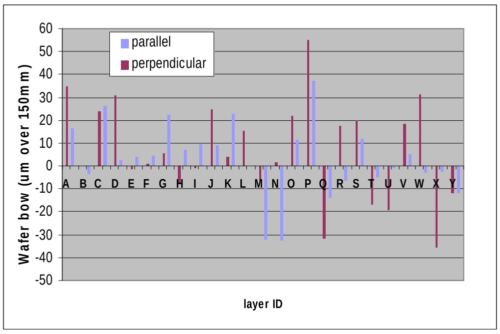

Figure 2 Measured bow before growth, over 150mm, parallel and perpendicular to wafer flat for the first batch of Si substrates.

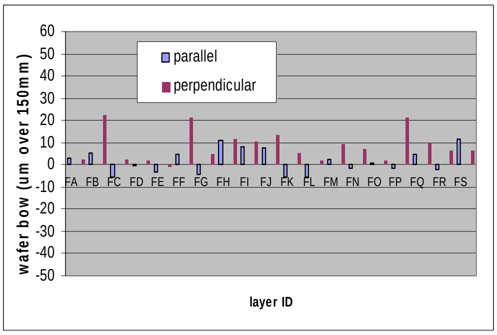

Figure 3 Measured bow over 150mm, before growth, parallel and perpendicular to the wafer flat for a batch of Si substrates from a second supplier.

	Wafer bow (µm)					
	Before growth		After growth		Net value	
Layer ID	90°	0°	90°	0°	90°	0°
Wafer 4	+10	+5	-30	-38	-40	-43
Wafer 5	+22	+5	-16	-29	-38	-34
Wafer 6	+21	+5	-20	-32	-41	-37
Wafer 7	-2	-1	-35	-40	-33	-39

Table 2 Wafer bow measured parallel (90°) and perpendicular (0°) to the wafer flat on bare 150mm substrates (before growth) and for GaN on Si structures (after growth). The final columns give the net bow introduced by the growth process.

The reproducibility of the growth process itself is shown in Table 2 which gives the starting bow before growth and final bow after growth of several 150mm wafers. The final columns give the net bow added during the growth process which is consistently below the target of 50µm.

Having established control of wafer bow on 150mm Si substrates, it is clearly also important to ensure that the electrical properties of the wafer are consistent with good device performance. Figure 4 shows an HgCV profile of a full FET structure on a 150mm Si substrate.

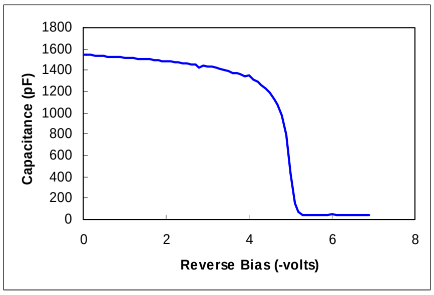

Figure 4 HgCV profile for a Full FET layer on a 150mm Si substrate.

The properties of the 2-Dimensional Electron Gas (2DEG) determined from this CV profile are a carrier density of $10\mathrm{x}10^{12}\mathrm{cm}^{-2}$, a V_{pinch} = -5.0Volts and t_{AlGaN} =24nm. These values are consistent with the layer specification defined in the EDA-funded KORRIGAN program for GaN HFET structures on SiC substrates. This wafer has a total bow (including initial Si bow) of -57µm and is consistent with a device specification suitable for processing at a commercial foundry.

Device Results

To demonstrate the potential device performance of a FET layer grown onto 150mm Si, a layer has been processed at QinetiQ using our standard device process as used for FETs on SiC substrates. The parameters measured on these devices are shown in table 3.

Parameter	Results
R_c (ohm.mm)	0.35
R_{sheet} (ohm / sq)	495±23
L_g (µm) (nominal)	0.25 µm T-gate
I_{dss0} (mA/mm)	605±17
g_m (mS/mm)	~250
V_p (V)	-3.88±0.18
Breakdown voltage (hard)	>100V
Gate leakage at 100V	<1 µA/mm

Table 3 Parameters measured on devices produced on a FET layer on 150mm Si.

The measured contact resistance of 0.35 ohm.mm and sheet resistance of 495 ohm/sq, along with I_{dss0}, g_m and V_p are all consistent with those expected from a similar structure on a SiC substrate. The devices also have excellent pinch-off, and high breakdown voltages and do not show any evidence of soft breakdown up to the maximum test voltage of 100Volts. A low value of f_T (7 GHz) was recorded on this wafer largely as a result of the highly conducting nature (~1 ohm-cm) of the Si (111) substrate used for growth. This conducting substrate material was used since at the outset of the programme a supplier of high resistivity 150mm Si could not be found to supply in research volumes to the required specification. However, a source of high resistivity substrates (>10kohm-cm) has recently been identified which meet the required specification and a batch of substrates purchased for assessment.

Conclusions

We have successfully demonstrated the growth of full HFET layers onto 150mm Si substrates with controlled wafer bow. These wafers are compatible with processing at commercial foundries in the UK. The device results obtained so far indicate that GaN on Si devices can deliver useful performance advantages over state-of-art GaAs devices for X-band applications and therefore provide a low cost route for GaN microwave technology to be made available for military and commercial applications. Work to address the performance of GaN on Si devices at high temperatures is on going.

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