Optimisation of AlGaN/GaN HEMTs Using Field Plates and Gate Recess Etching

R.T. Green (1), K.B. Lee (1), I.J. Luxmoore (1), P.A. Houston (1), M.J Uren (2), D.J Wallis (2), and T. Martin (2)
(1) Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield, S1 3JD, UK.
(2) QinetiQ Ltd, St. Andrews Road, Great Malvern, Worcestershire WR14 3PS, UK.

Abstract

Incorporating GaN capping layers in conjunction with gate recessing and/or field plates has been identified as a means to maximise the high frequency performance of AlGaN/GaN HEMTs. Using either a $SiCl_4/SF_6$ or $Cl_2/Ar/O_2$ dry etch plasma recipe, self-aligned gate recess HEMTs were fabricated. The $SiCl_4/SF_6$ dry etch plasma chemistry was found to introduce minimal damage to the semiconductor during the recess process. Incorporation of field plates into standard AlGaN/GaN structures increased breakdown voltage by up to 70% and reduced RF dispersion effects.

Introduction

Due to a high band gap, large breakdown voltage, high saturation velocity and large sheet charge concentration, AlGaN/GaN high electron mobility transistors (HEMTs) have been identified as promising candidates for high power, high temperature devices operating at microwave frequencies. Large signal RF performance in these components is currently limited by surface and bulk charge trapping states in the material structure [1] and also parasitic elements associated with the source and drain access resistances [2]. The use of field plates in GaN-based transistors enhances DC and RF performance by improving the breakdown voltage and by moderating the electric field at the AlGaN surface leading to reduced dispersion [3]. Gate-terminated field plate geometries have led to impressive output power densities of up to $40Wmm^{-1}$ at 8GHz [4], which are made possible primarily due to the increased breakdown voltage. This geometry, however, leads to increased gate-drain feedback capacitance and reduced gain. Gate recessing using GaN capping layers has been demonstrated as a mechanism to increase gain, achieving improved power performance [5] and reduced parasitic contact resistances [6]. The design of the cap is critical since the polarisation charge, due to the addition of the upper GaN film, can reduce the number of carriers in the 2-dimensional electron gas (2DEG) resulting in increased access resistance [7].

To minimise leakage currents and maximise gain in GaN/AlGaN/GaN structures, the gate must be recessed through the upper GaN layer using a suitable selective etching process. Standard Cl_2/Ar dry etch plasma chemistries have negligible selectivity between GaN and AlGaN [8] and, due to issues relating to both surface and plasma etch conditions, the recess depth is susceptible to variation [9]. For GaN-capped devices, $Cl_2/Ar/O_2$ [10], BCl_3/SF_6 [11] and $SiCl_4/SF_6$-based [12] recipes are able to provide an effective etch stop leading to improved depth control. Despite the continued use of these dry etch recipes little has been reported regarding damage to the underlying semiconductor after exposure to the plasma.

This paper is split into two distinct sections. Firstly, experimental results for gate recessed Schottky diode test structures and HEMTs fabricated using a selective $Cl_2/Ar/O_2$ or $SiCl_4/SF_6$ dry etch plasma chemistry are presented. Room temperature and temperature dependent I-V characteristics are subsequently used to compare damage introduced into the structures. Secondly, results on field plates on standard AlGaN/GaN HEMTs are presented and their performance examined using pulse bias measurements to simulate large signal RF operation.

Separately optimising gate recessing methodologies and field plate geometries will enable the realisation of devices with significantly improved RF performance.

Experimental

AlGaN/GaN and GaN/AlGaN/GaN structures were grown by metal-organic vapour phase epitaxy (MOVPE) on 2 inch sapphire substrates. Initially a 2μm semi-insulating GaN buffer layer was grown followed by a 22nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer. For capped structures, an analytical model was used to design the optimum structure which incorporated a highly n^+ doped ($\sim 5\times10^{19}cm^{-3}$) 5nm thick GaN layer. For all structures, the group III precursors used were trimethylgallium (TMG) and trimethylaluminium (TMA) and the group V precursor was ammonia (NH_3). N-type doping was achieved through the introduction of silane (SiH_4).

To fabricate the transistors and large area Schottky diodes the following procedures were employed. Device isolation was achieved using low RF power inductively coupled plasma (ICP) etching using a $SiCl_4/Cl_2/Ar$ recipe. Ti/Al/Ti/Au (20/100/45/55nm) ohmic contacts were deposited and annealed at 800°C for 30 seconds under N_2. Ni/Au (20/100nm) and Ti/Au (20/200nm) metals were used to form gate and ohmic bond pads respectively. For recessed devices the gate was defined using electron beam lithography (EBL) and gate recessing was performed in a self-aligned step with resist acting as the etch mask. Ni/Au (20nm/100nm) was used for the gate metallisation. Recessing was achieved using either a $Cl_2/Ar/O_2$ or $SiCl_4/SF_6$ dry etch recipe, the latter of which was developed by our group at Sheffield [12]. The $SiCl_4/SF_6$ recipe used a pressure of 50mTorr and flow rates of 20 and 5sccm for $SiCl_4$ and SF_6 respectively. For the $Cl_2/Ar/O_2$ recipe, flow rates of 30, 10 and 2sccm respectively were used in conjunction with a pressure of 10mTorr [13]. For both recipes the ICP power was set to 450W, the RF power was 50W and the table temperature set to 20°C. For non-recessed devices a single stage of EBL was used to define the gate with the selective recessing stage omitted. For devices which incorporated a field plate, the gate was initially deposited using EBL followed by deposition of SiN to various thicknesses ranging from 100nm to 500nm using a plasma enhanced chemical vapour deposition (PECVD) system. A second stage of EBL was used to define the Ni/Au (20nm/100nm) field plate which was connected to the gate extrinsically from the device.

Results

I. Gate Recessing

HEMT characteristics for a recessed gate device and a device with the gate deposited directly on top of the GaN cap (non-recessed) are shown in figure 1. A clear decrease in pinch-off voltage from ~2.8V to ~1.9V was observed for the non-recessed and recessed device respectively, which can be attributed to the decrease in gate-channel separation. An increase in maximum transconductance from $\sim180mSmm^{-1}$ to $\sim200mSmm^{-1}$ is also observed revealing the increase in gain made possible via the recessing process. Transmission line measurements (TLM) revealed sheet resistances of 570Ω/□ and 510Ω/□ for capped and un-capped structures respectively. The 2DEG mobility was found to increase from 1100 $cm^2V^{-1}s^{-1}$ for standard uncapped devices to $1300cm^2V^{-1}s^{-1}$ for capped HEMT structures. Contact resistances were reduced from 0.8Ωmm to 0.3Ωmm for metals deposited on standard and capped material respectively. This significant reduction in contact resistance demonstrates the effectiveness of utilising GaN capping layers in order to reduce parasitics in the HEMT structure to maximise RF performance. The non-recessed device has a maximum output current of $540mAmm^{-1}$, which decreases to $400mAmm^{-1}$ after recessing. Although not shown here, devices recessed using the $Cl_2/Ar/O_2$ recipe show a similar reduction in output current. It has been suggested that exposing GaN-based materials to ionising plasmas can result in the creation of acceptor-like states into the near surface region of the semiconductor [14]. In AlGaN/GaN HEMTs this would result in a reduction in 2DEG density. We propose a similar model, whereby shallow states have been introduced into the AlGaN, which depletes carriers from the channel.

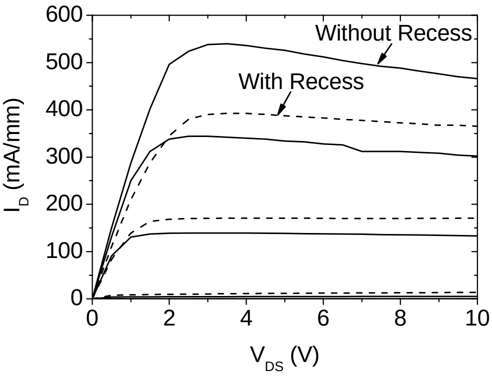

Figure 1 – DC characteristics for recessed and non-recessed HEMT devices. The gate-source voltage for both devices was biased from 0V to -4V in steps of 1V.

Bulk leakage components for large area, reverse-biased Schottky diodes revealed that for devices recessed using the $SiCl_4/SF_6$ plasma chemistry the bulk leakage current has been reduced by 1-2 orders of magnitude when compared to non-recessed devices or transistors recessed using the O_2-based recipe. Temperature dependent measurements of the forward bias (DC) characteristics revealed metal-semiconductor barrier heights of 0.45eV and 1eV for devices recessed using the $Cl_2/Ar/O_2$ and $SiCl_4/SF_6$ recipe respectively. This demonstrates that the $SiCl_4/SF_6$ recipe gives superior characteristics when compared to other O_2-based selective etch recipes.

It is widely believed that electrons contained within the 2DEG are supplied to the channel via surface states [15] and that this charge is contained in the GaN buffer at the heterointerface by spontaneous and piezoelectric polarisation. The number of electrons in the channel region is further augmented by electrically active ionised impurity concentrations contained within the AlGaN barrier. Since the number of channel electrons supplied by surface states is insensitive to temperature and the barrier layer is nominally undoped, the variation in threshold voltage as a function of temperature can be used to give a measure of the number of electrically active trapping states (temperature sensitive) below the gate metal. The temperature dependent shift in threshold voltage for recessed and non-recessed devices is shown in figure 2. For recessed devices there is a clear change in threshold voltage due to the difference in gate-channel separation. However, the threshold voltages for both the non-recessed devices and devices recessed using the $Cl_2/Ar/O_2$ recipe show significantly greater dependence on operating temperature when compared to transistors recessed using the $SiCl_4/SF_6$ plasma, indicating fewer bulk trapping states for the latter.

This further confirms the effectiveness of using the $SiCl_4/SF_6$ etch recipe in the fabrication of gate recessed GaN-based HEMTs.

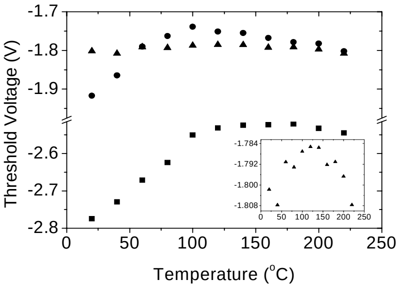

Figure 2 – (a) Threshold voltage as a function of temperature for a non-recessed n^+GaN capped HEMT (■), an n^+GaN capped HEMT recessed using a $SiCl_4/SF_6$ (▲) or $Cl_2/Ar/O_2$ (●) plasma recipe. Inset in shows magnified scale of threshold change for devices recessed using the $SiCl_4/SF_6$ plasma recipe.

II. Field Plates

The electric field in the channel region of a HEMT will peak at the drain edge of the gate. By incorporating a field plate, a second peak in the electric field is formed which spreads the voltage drop, leading to a moderation in the maximum electric field. A cross sectional image of a completed HEMT structure incorporating a gate terminated field plate is shown in figure 3. The extension of the plate is defined as the distance between the drain edge side of the gate and the edge of the field plate.

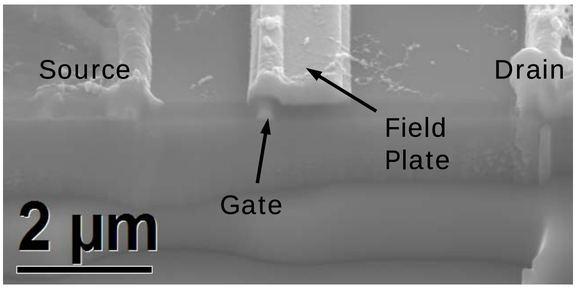

Figure 3 – Cross section of a HEMT device incorporating a field plate structure.

The corresponding 3-terminal breakdown voltage (with the gate-source voltage held at pinch off) for gate terminated devices is shown in figure 4. Incorporating a 1.5µm extension in conjunction with a standard AlGaN/GaN HEMT resulted in an increase in breakdown voltage from ~35V to ~55V representing a ~70% improvement at pinch off. However, in this test case the field plate is close to the drain (≤2µm) leading to an overall reduced breakdown voltage for devices with field plates >1.5µm [16]. Modelling of the reduction in f_T for field plated HEMTs reveals that devices utilising a 1µm field plate with a 500nm SiN layer should show a reduction in f_T of ~15%. RF measurements performed on these devices revealed a unity gain cut-off frequency of ~20GHz indicating their suitability for high power X-band applications. By decreasing the thickness of the dielectric layer from 500nm to 200nm the breakdown voltage was not improved. However, the theoretical f_T is reduced by ~25% in this case, representing an unacceptably large degradation in frequency response.

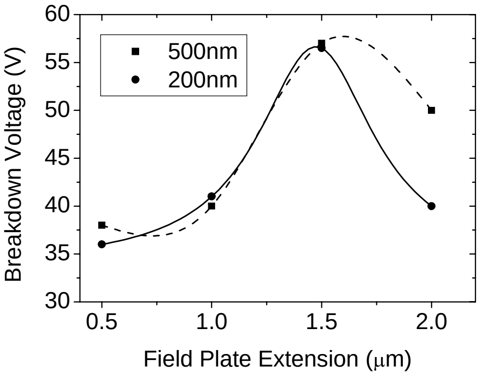

Figure 4 – Breakdown voltages measured for AlGaN/GaN HEMTs with varying dielectric thickness and field plate extensions. The gate-source voltage was set at -7V.

Current dispersion measurements were employed to characterise these devices whereby the gate is biased at pinch off and the drain-source voltage is set at a figure which is indicative of a typical maximum operating value (in this case 20V). Both the gate and drain are then pulsed to full channel current using a 1µs pulse width. This value is then compared to the dc figure to give an indication of dispersion. The normalised current dispersions for various gate-terminated field plate structures utilising varying SiN thickness and field plate extension are compared in figure 5.

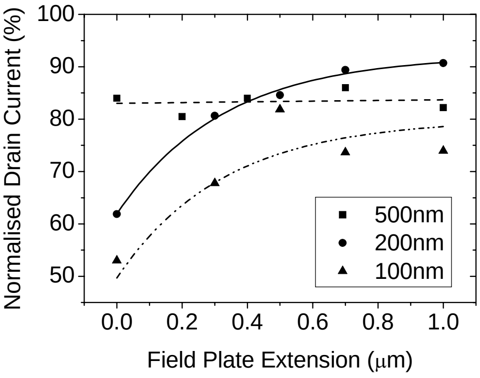

Figure 5 – Current dispersion measured using a dual pulse setup for varying SiN thicknesses and field plate extensions.

Generally, as the field plate extension increases, the degree of RF dispersion in the component is found to reduce. Modelling of this geometry shows that the maximum field at the gate edge is reduced with increasing field plate extension, leading to a reduction in charge trapping at the AlGaN surface. However, at large extension lengths this effect will saturate as the field becomes evenly split between the gate and field plate, after which any further increase in the plate extension will not improve breakdown but will simply add to parasitic gate capacitances [17]. Furthermore, the effectiveness of the field plate to influence current dispersion in the devices is found to reduce for increasing SiN thickness. Since the field modulating plate influences the channel via a capacitive action, this is consistent with the plate being physically further from the channel.

All devices fabricated without field plates show different degrees of dispersion which is inconsistent with our presented model. This is believed to be due to variations in processing which alter the effectiveness of the SiN to reduce RF dispersion and has been widely observed by other groups.

Conclusions

An n^+GaN capping layer is advantageous since it leads to reduced contact resistances associated with the drain and source. Devices recessed using a $SiCl_4/SF_6$ etch recipe has been shown to demonstrate improved characteristics when compared to O_2-based plasmas. Capped structures greatly reduced the parasitic contact resistances which will lead to improved high frequency performance. The recessed devices show degradation in output current compared to non-recessed devices, but significantly reduced charge trapping effects. Field plates have also been employed to increase breakdown voltage in AlGaN/GaN HEMTs by up to ~70% for devices with a 1.5µm extension field plate and a 500nm thick SiN dielectric layer. This same structure is found to significantly reduce RF dispersion without significantly degrading f_T. Incorporating either or both these technologies into GaN-based HEMTs will therefore yield significant improvements when operating devices under large signal RF conditions.

Acknowledgements

The work reported in this paper was funded by the Electro-magnetic Remote Sensing (EMRS) Defence Technology Centre, established by the UK Ministry of Defence and run by a consortium of SELEX Galileo, Thales UK and Roke Manor Research.

References

1. R. Vetury et al, “The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs” *IEEE Trans Electron Dev*, Vol. 48, pp 560-566, 2001
2. Nidhi et al, “Study of impact of access resistance on high-frequency performance of AlGaN/GaN HEMTs by measurement at low temperature” *IEEE Electron Dev Lett*, Vol. 27, pp 877-880, 2006
3. S. Karmalkar et al, “Field-plate engineering for HFETs” *IEEE Trans Electron Dev*, Vol. 52, pp 2534-2540, 2005
4. Y.F. Wu et al, “40-W/mm double field-plated GaN HEMTs” *IEEE 64th Device Research Conference*, pp 151-152, 2006
5. Y. Pei et al, “Effect of Al composition and gate recess on power performance of AlGaN/GaN high electron mobility transistors” *IEEE Electron Dev Lett*, Vol. 29, pp 300-302, 2008
6. Y. Pei et al, “Study of the n^+ GaN cap in AlGaN/GaN high electron mobility transistors with reduced source-drain resistance” *Jpn J of Appl Phys*, Vol. 46, pp L842-844, 2007
7. S. Heikman et al, “Polarisation effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures” *J Appl Phys*, Vol. 93, pp 10114-10118, 2003
8. D. Buttari et al, “Origin of etch delay time in Cl_2 dry etching of AlGaN/GaN structures” *Appl Phys Lett*, Vol. 83, pp 4779-4781, 2003
9. J.S. Moon et al, “Gate-recessed AlGaN-GaN HEMTs for high-performance millimetre-wave applications” *IEEE Electron Dev Lett*, Vol. 26, pp 348-350, 2005
10. J.M. Lee et al, “Inductively coupled $Cl_2/Ar/O_2$ plasma etching of GaN, InGaN and AlGaN” *Journal of Korean Physical Society*, Vol. 37, pp 842-845, 2000
11. D. Buttari et al, “Selective dry etching of GaN over AlGaN in BCl_3/SF_6 mixture” *Proceedings of the 2004 IEEE Lester Eastman Conference on High Performance Devices*, pp 132-137, 2004
12. R.T. Green et al, “Comparison of damage introduced into GaN/AlGaN/GaN heterostructures using selective dry etch recipes” Submitted to *Semiconductor Science and Technology*, 2009
13. J.M. Lee et al, “Highly selective dry etching of III nitrides using an inductively coupled $Cl_2/Ar/O_2$ plasma” *J Vac Sci Tech B*, vol. 18, pp 1409-1411, 2000
14. R. Chu et al, “Impact of CF_4 plasma treatment on GaN” *IEEE Electron Dev Lett*, Vol. 28, pp 781-783, 2007
15. J.P. Ibbetson et al, “Polarisation effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors” *Appl Phys Lett*, Vol. 77, pp 250-252, 2000
16. Y.F. Wu et al, “30-W/mm GaN HEMTs by field plate optimization” *IEEE Electron Dev Lett*, Vol. 25, pp 117-119, 2004
17. S. Karmalkar and U.K. Mishra “Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate” *IEEE Trans Electron Dev*, Vol. 48, pp 1515-1521, 2001